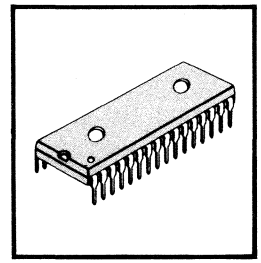
SAMSUNG

Data Book

MOS Memory

Vol. 2 1992/93



- SRAM
- FIFO

PRINTED IN KOREA

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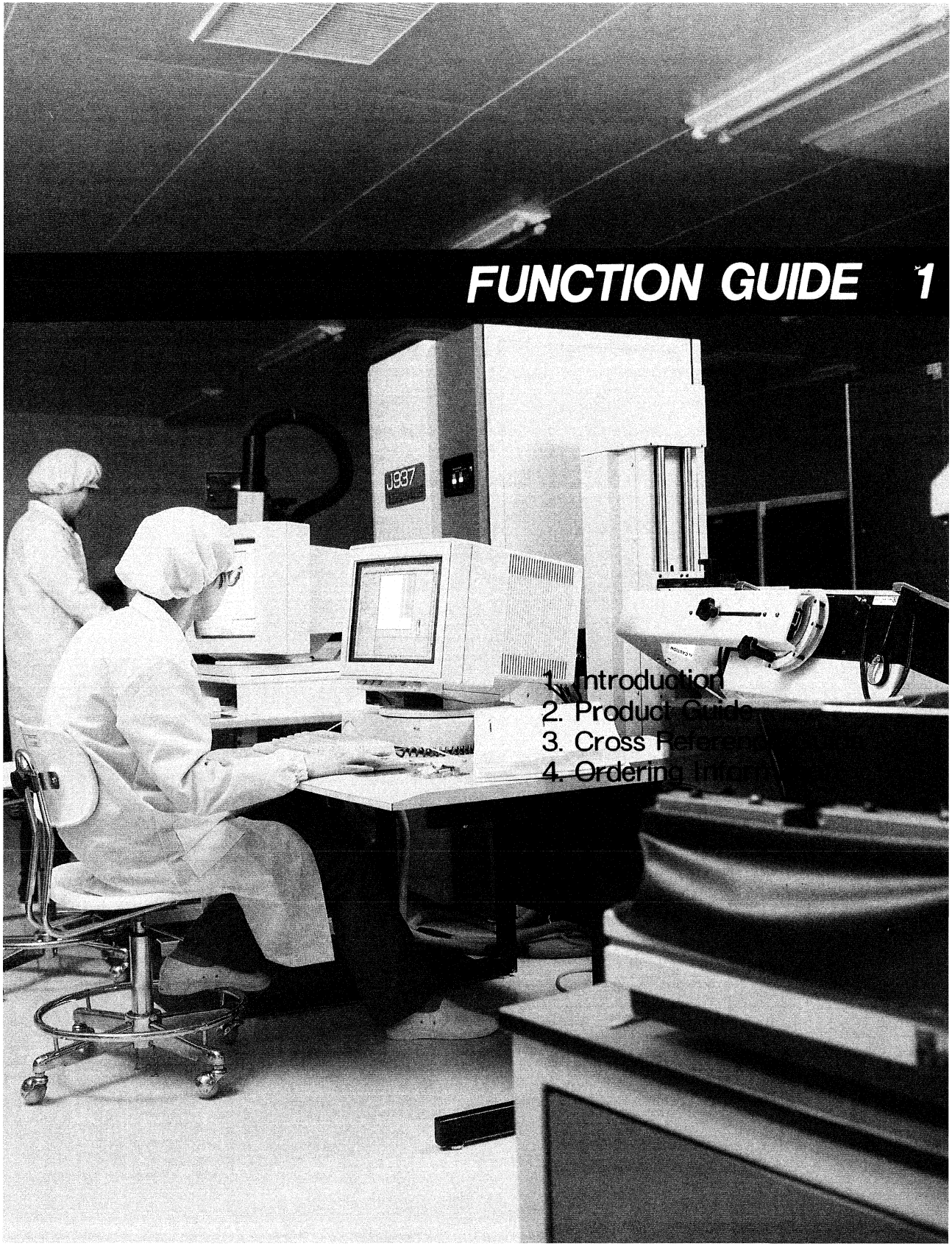
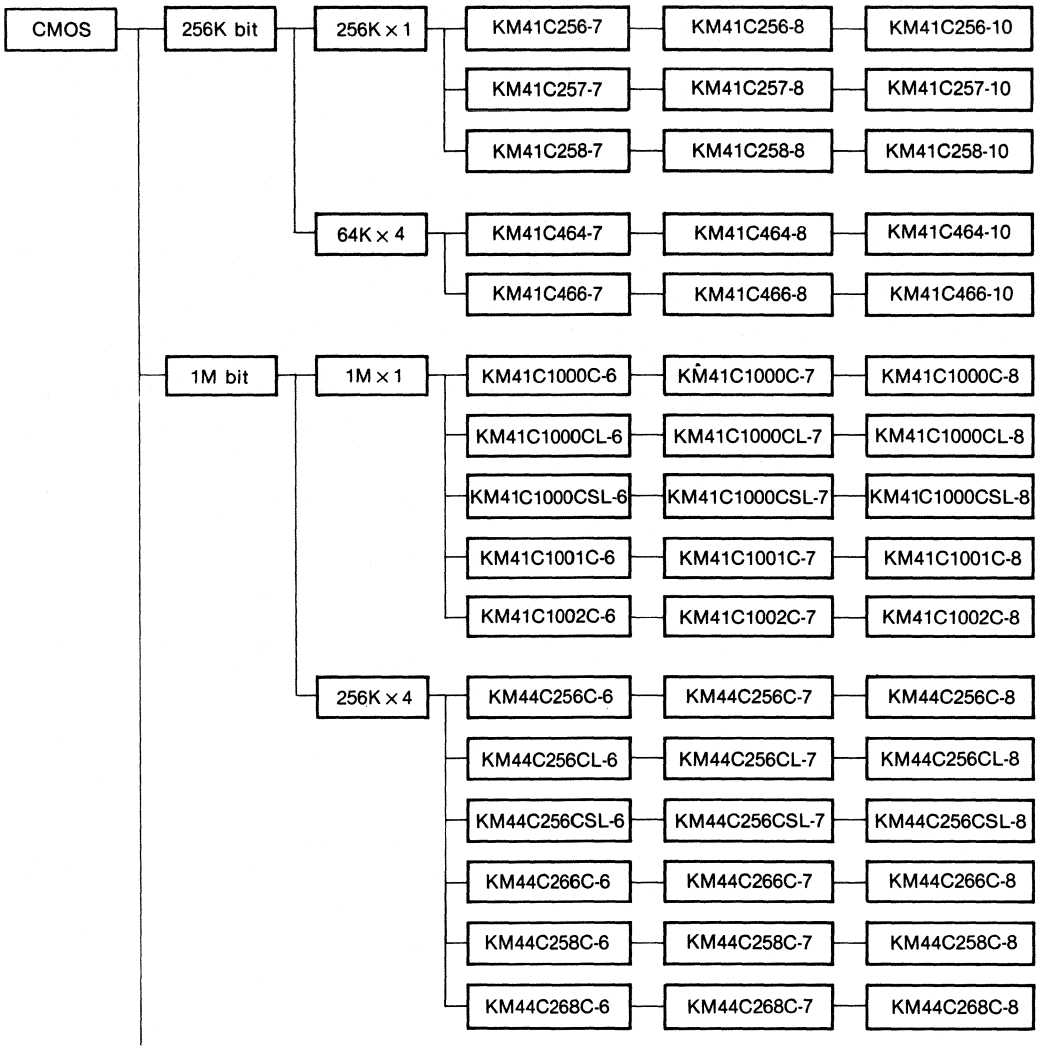


1. INTRODUCTION

1.1 Dynamic RAM



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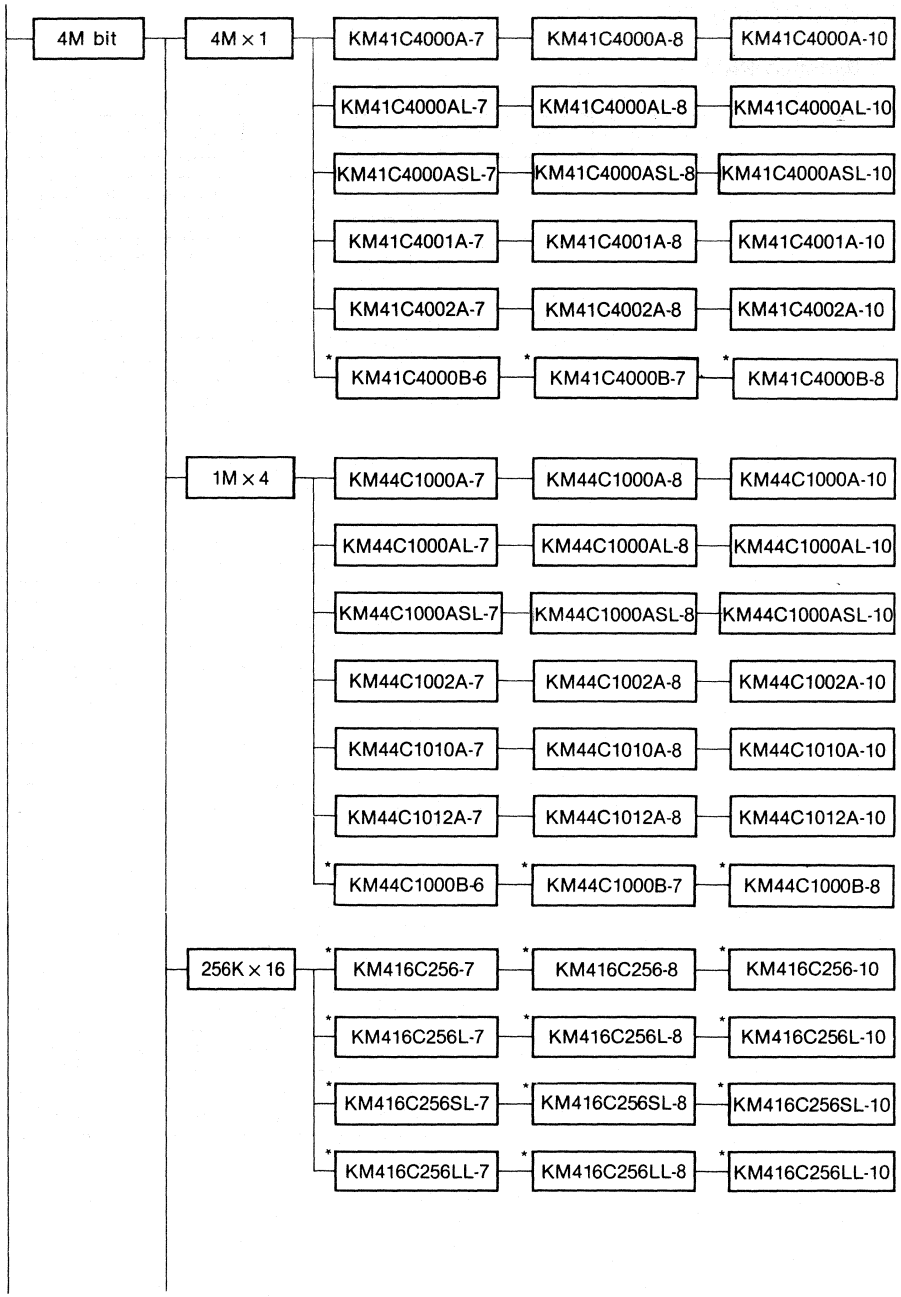
4M bit
4M × 1
KM41C4000A-7
KM41C4000A-8
KM41C4000A-10
KM41C4000AL-7
KM41C4000AL-8
KM41C4000AL-10
KM41C4000ASL-7
KM41C4000ASL-8
KM41C4000ASL-10
KM41C4001A-7
KM41C4001A-8
KM41C4001A-10
KM41C4002A-7
KM41C4002A-8
KM41C4002A-10
*KM41C4000B-6
*KM41C4000B-7
*KM41C4000B-8
1M × 4
KM44C1000A-7
KM44C1000A-8
KM44C1000A-10
KM44C1000AL-7
KM44C1000AL-8
KM44C1000AL-10
KM44C1000ASL-7
KM44C1000ASL-8
KM44C1000ASL-10
KM44C1002A-7
KM44C1002A-8
KM44C1002A-10
KM44C1010A-7
KM44C1010A-8
KM44C1010A-10
KM44C1012A-7
KM44C1012A-8
KM44C1012A-10
*KM44C1000B-6
*KM44C1000B-7
*KM44C1000B-8
256K × 16
*KM416C256-7
*KM416C256-8
*KM416C256-10
*KM416C256L-7
*KM416C256L-8
*KM416C256L-10
*KM416C256SL-7
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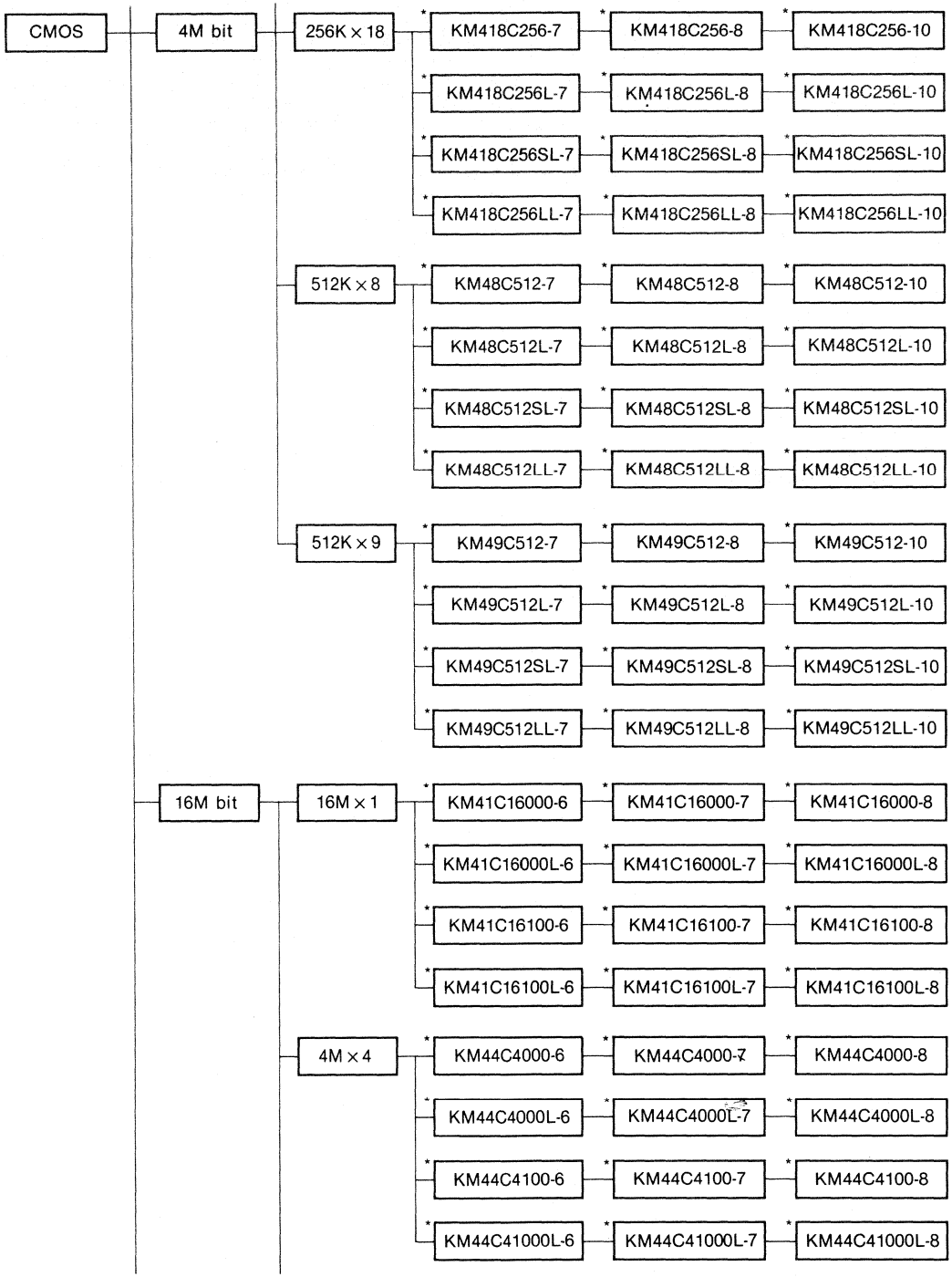
*KM416C256LL-7
*KM416C256LL-8
*KM416C256LL-10


CMOS
4M bit
256K × 18
KM418C256-7
KM418C256-8
KM418C256-10
KM418C256L-7
KM418C256L-8
KM418C256L-10
KM418C256SL-7
KM418C256SL-8
KM418C256SL-10
KM418C256LL-7
KM418C256LL-8
KM418C256LL-10
512K × 8
KM48C512-7
KM48C512-8
KM48C512-10
KM48C512L-7
KM48C512L-8
KM48C512L-10
KM48C512SL-7
KM48C512SL-8
KM48C512SL-10
KM48C512LL-7
KM48C512LL-8
KM48C512LL-10
512K × 9
KM49C512-7
KM49C512-8
KM49C512-10
KM49C512L-7
KM49C512L-8
KM49C512L-10
KM49C512SL-7
KM49C512SL-8
KM49C512SL-10
KM49C512LL-7
KM49C512LL-8
KM49C512LL-10
16M bit
16M × 1
KM41C16000-6
KM41C16000-7
KM41C16000-8
KM41C16000L-6
KM41C16000L-7
KM41C16000L-8
KM41C16100-6
KM41C16100-7
KM41C16100-8
KM41C16100L-6
KM41C16100L-7
KM41C16100L-8
4M × 4
KM44C4000-6
KM44C4000-7
KM44C4000-8
KM44C4000L-6
KM44C4000L-7
KM44C4000L-8
KM44C4100-6
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KM44C41000L-7
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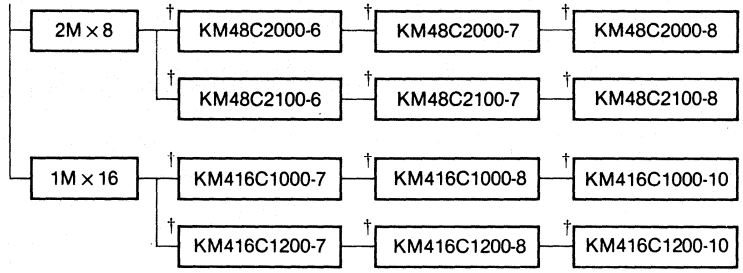
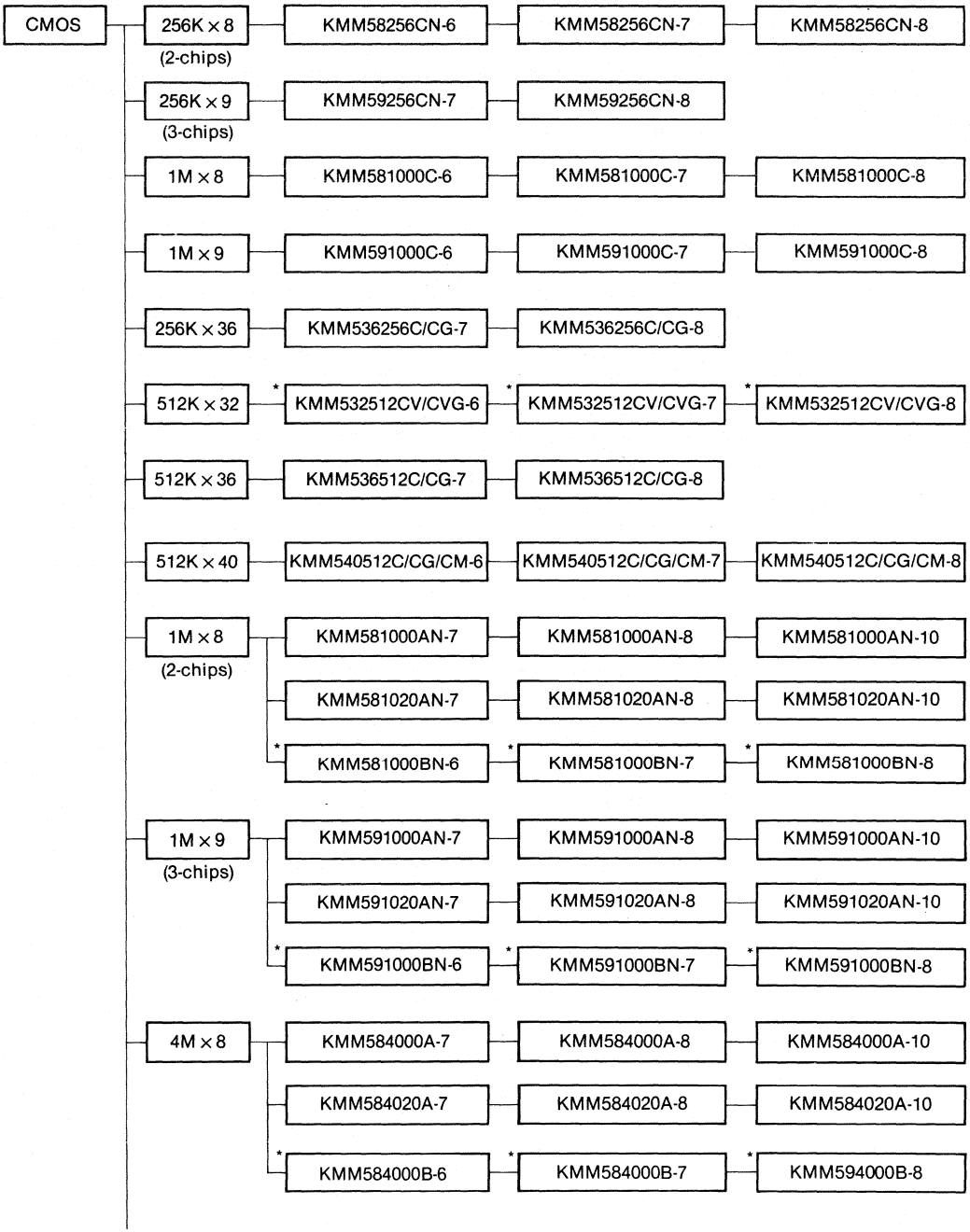
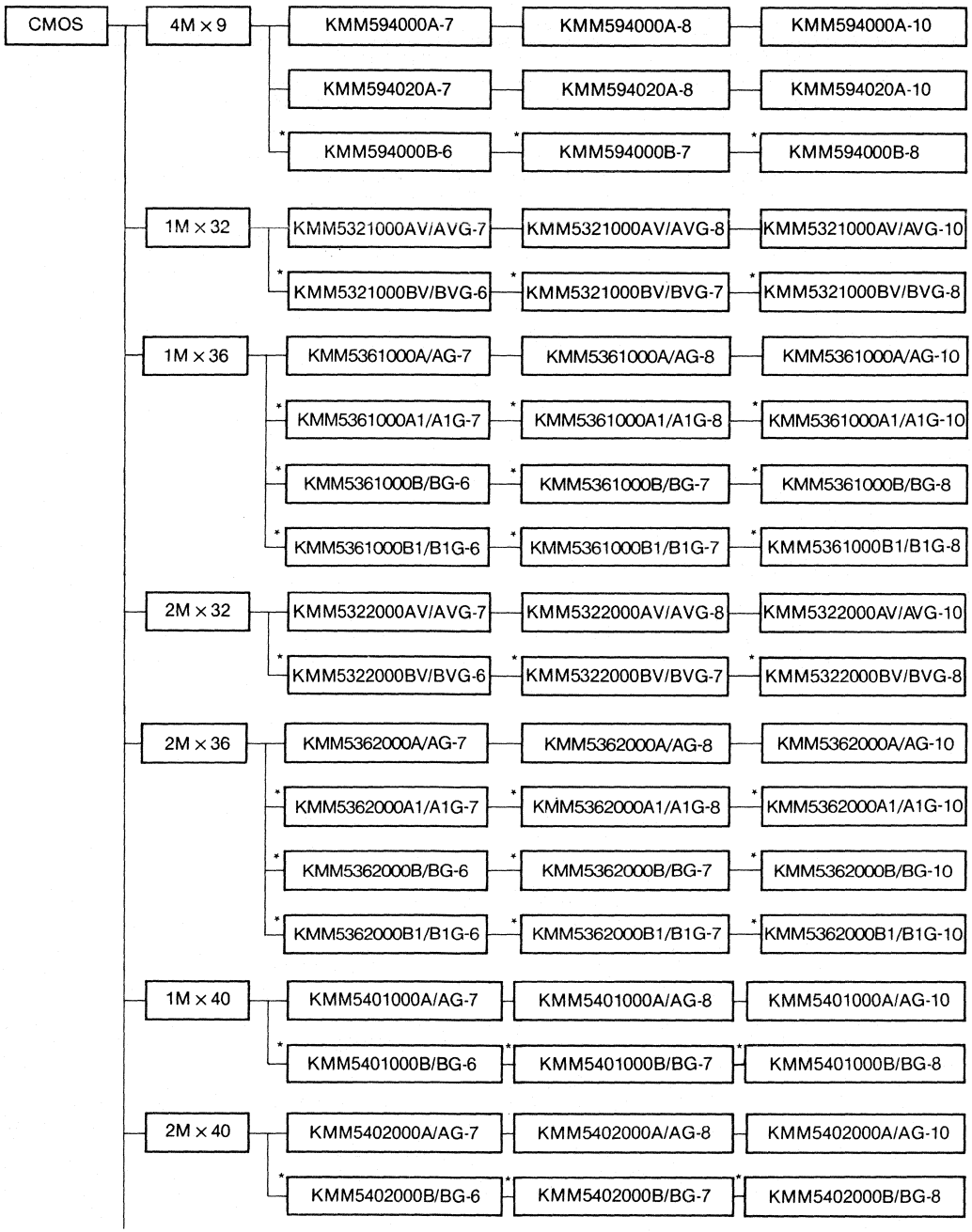
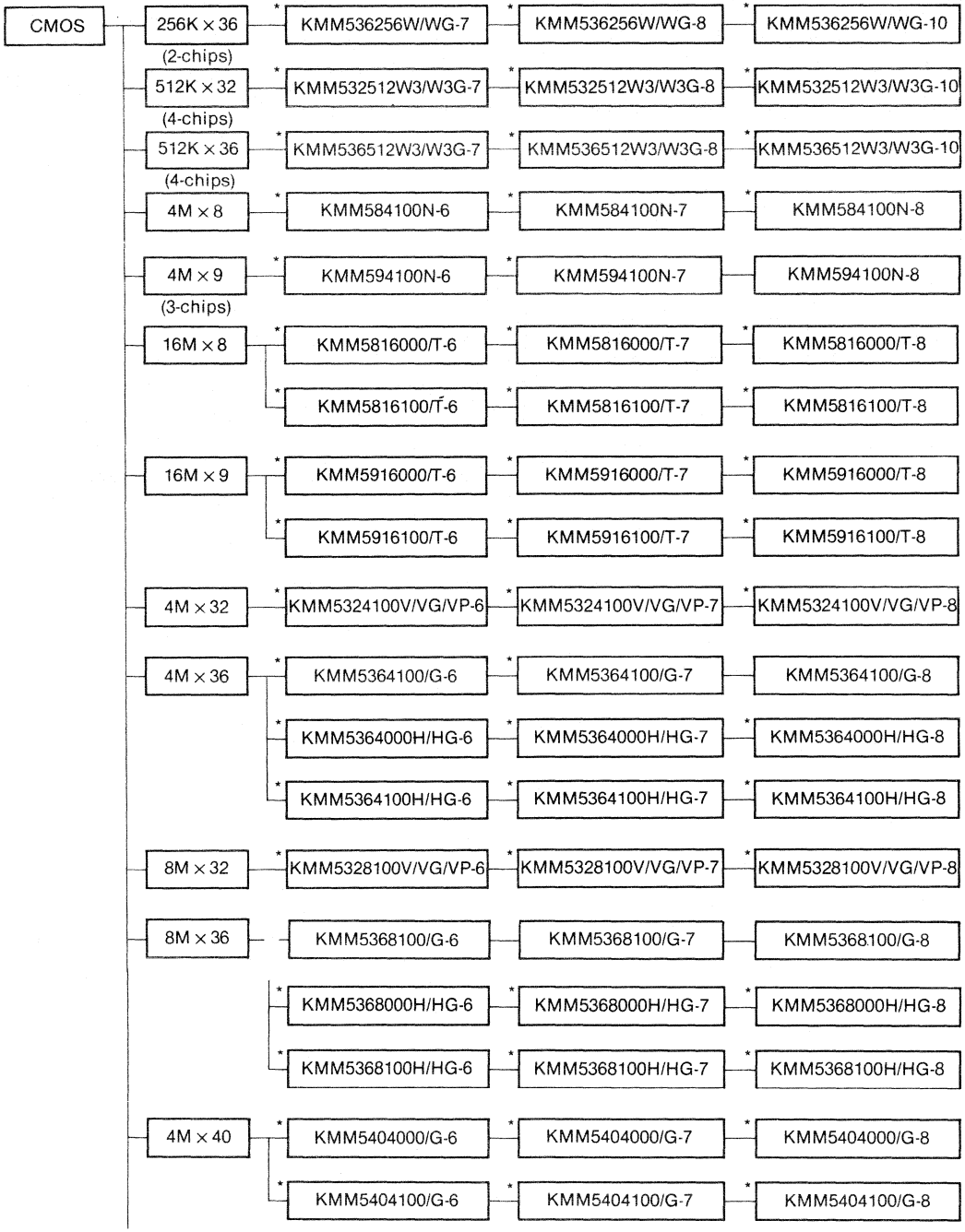


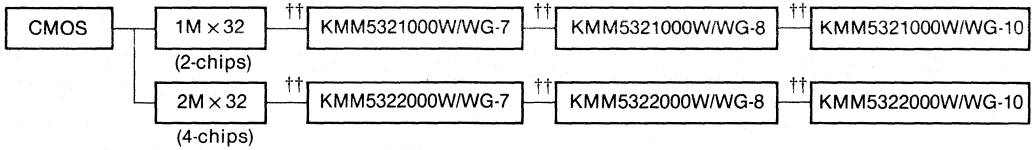
*: New Product
†: Preliminary Product
††: Under Development

1.2 Dynamic RAM Module



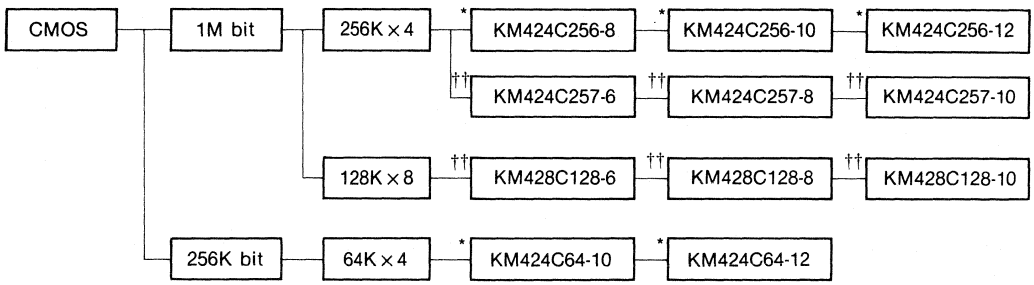

CMOS
4M × 9
KMM594000A-7
KMM594000A-8
KMM594000A-10
KMM594020A-7
KMM594020A-8
KMM594020A-10
*KMM594000B-6
*KMM594000B-7
*KMM594000B-8
1M × 32
KMM5321000AV/AVG-7
KMM5321000AV/AVG-8
KMM5321000AV/AVG-10
*KMM5321000BV/BVG-6
*KMM5321000BV/BVG-7
*KMM5321000BV/BVG-8
1M × 36
KMM5361000A/AG-7
KMM5361000A/AG-8
KMM5361000A/AG-10
*KMM5361000A1/A1G-7
*KMM5361000A1/A1G-8
*KMM5361000A1/A1G-10
*KMM5361000B/BG-6
*KMM5361000B/BG-7
*KMM5361000B/BG-8
*KMM5361000B1/B1G-6
*KMM5361000B1/B1G-7
*KMM5361000B1/B1G-8
2M × 32
KMM5322000AV/AVG-7
KMM5322000AV/AVG-8
KMM5322000AV/AVG-10
*KMM5322000BV/BVG-6
*KMM5322000BV/BVG-7
*KMM5322000BV/BVG-8
2M × 36
KMM5362000A/AG-7
KMM5362000A/AG-8
KMM5362000A/AG-10
*KMM5362000A1/A1G-7
*KMM5362000A1/A1G-8
*KMM5362000A1/A1G-10
*KMM5362000B/BG-6
*KMM5362000B/BG-7
*KMM5362000B/BG-10
*KMM5362000B1/B1G-6
*KMM5362000B1/B1G-7
*KMM5362000B1/B1G-10
1M × 40
KMM5401000A/AG-7
KMM5401000A/AG-8
KMM5401000A/AG-10
*KMM5401000B/BG-6
*KMM5401000B/BG-7
*KMM5401000B/BG-8
2M × 40
KMM5402000A/AG-7
KMM5402000A/AG-8
KMM5402000A/AG-10
*KMM5402000B/BG-6
*KMM5402000B/BG-7
*KMM5402000B/BG-8


CMOS
256K × 36
(2-chips)
KMM536256W/WG-7
KMM536256W/WG-8
KMM536256W/WG-10
512K × 32
(4-chips)
KMM532512W3/W3G-7
KMM532512W3/W3G-8
KMM532512W3/W3G-10
512K × 36
(4-chips)
KMM536512W3/W3G-7
KMM536512W3/W3G-8
KMM536512W3/W3G-10
4M × 8
KMM584100N-6
KMM584100N-7
KMM584100N-8
4M × 9
(3-chips)
KMM594100N-6
KMM594100N-7
KMM594100N-8
16M × 8
KMM5816000/T-6
KMM5816000/T-7
KMM5816000/T-8
KMM5816100/T-6
KMM5816100/T-7
KMM5816100/T-8
16M × 9
KMM5916000/T-6
KMM5916000/T-7
KMM5916000/T-8
KMM5916100/T-6
KMM5916100/T-7
KMM5916100/T-8
4M × 32
KMM5324100V/VG/VP-6
KMM5324100V/VG/VP-7
KMM5324100V/VG/VP-8
4M × 36
KMM5364100/G-6
KMM5364100/G-7
KMM5364100/G-8
KMM5364000H/HG-6
KMM5364000H/HG-7
KMM5364000H/HG-8
KMM5364100H/HG-6
KMM5364100H/HG-7
KMM5364100H/HG-8
8M × 32
KMM5328100V/VG/VP-6
KMM5328100V/VG/VP-7
KMM5328100V/VG/VP-8
8M × 36
KMM5368100/G-6
KMM5368100/G-7
KMM5368100/G-8
KMM5368000H/HG-6
KMM5368000H/HG-7
KMM5368000H/HG-8
KMM5368100H/HG-6
KMM5368100H/HG-7
KMM5368100H/HG-8
4M × 40
KMM5404000/G-6
KMM5404000/G-7
KMM5404000/G-8
KMM5404100/G-6
KMM5404100/G-7
KMM5404100/G-8



* New Product
†† Under Development

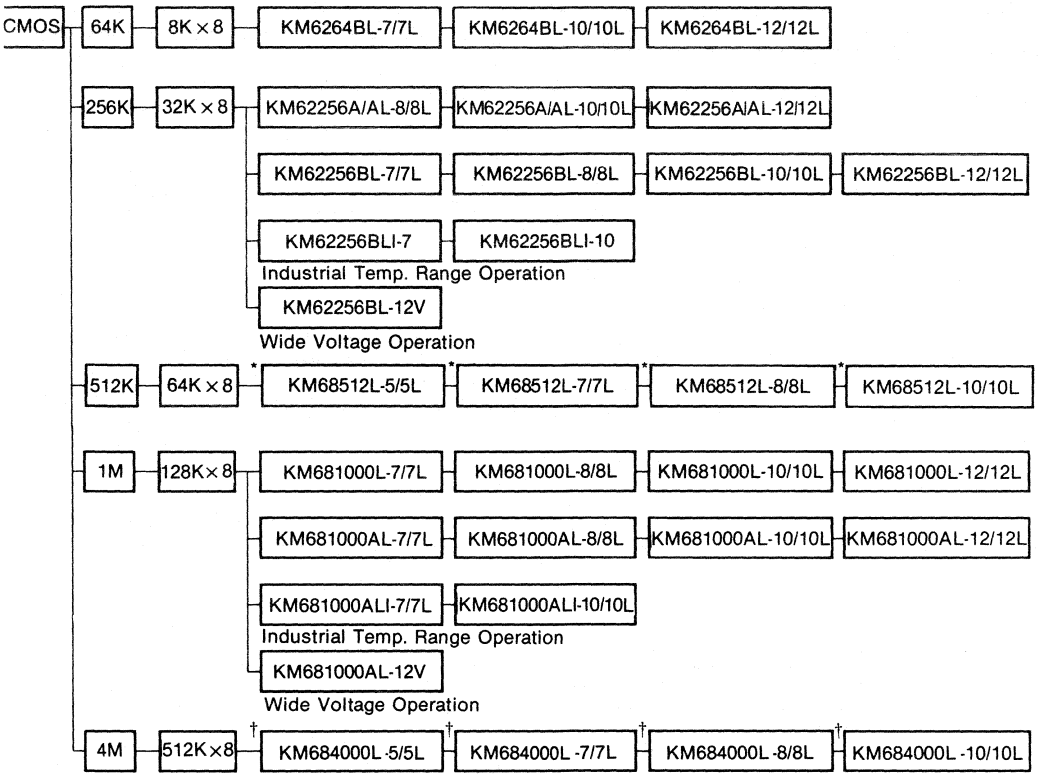
1.3 Video RAM



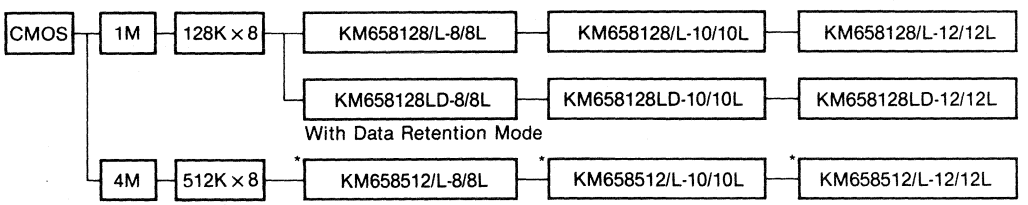
*: New Product
†: Preliminary Product
††: Under Development

1.4 Static RAM

Low Power SRAMs

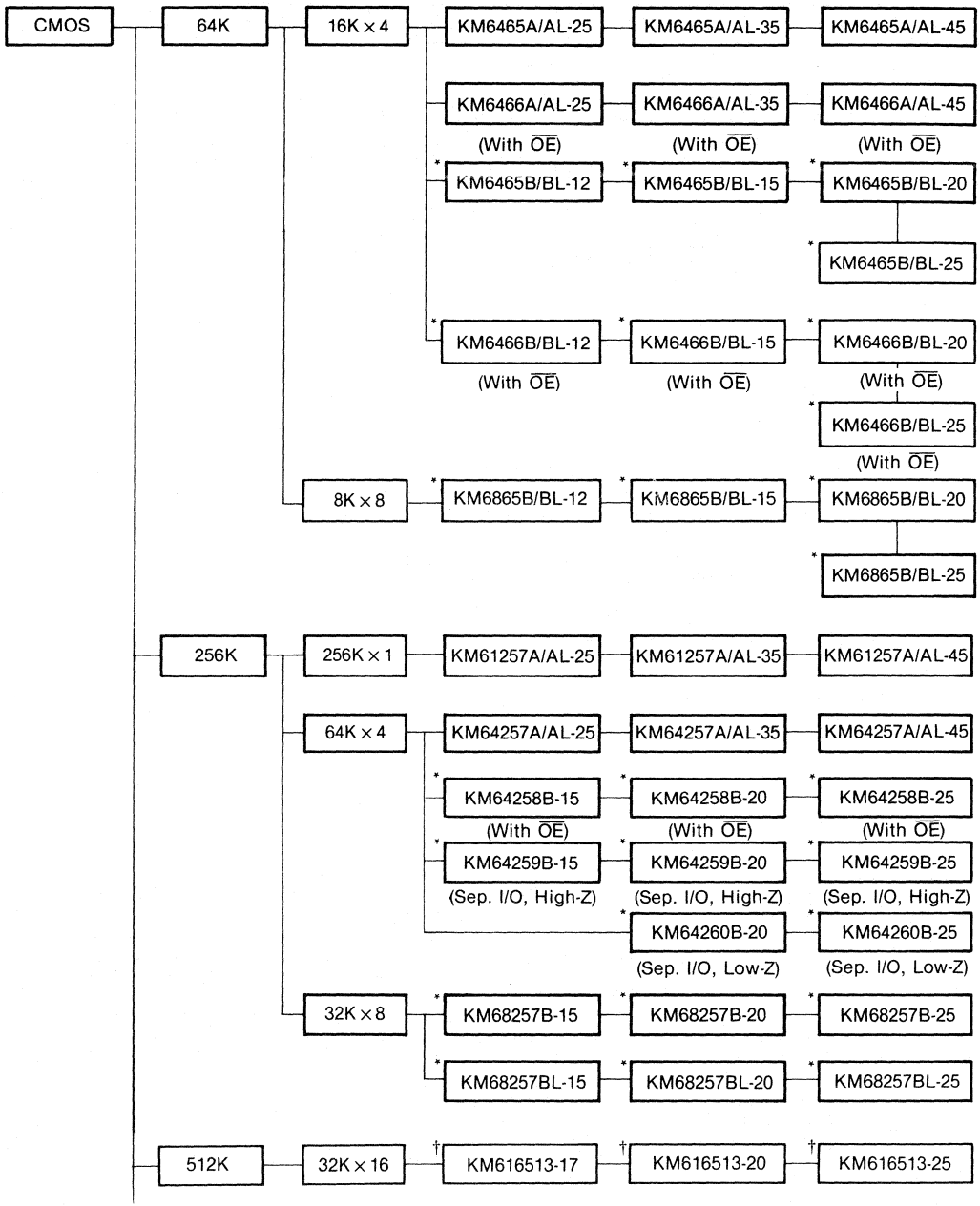


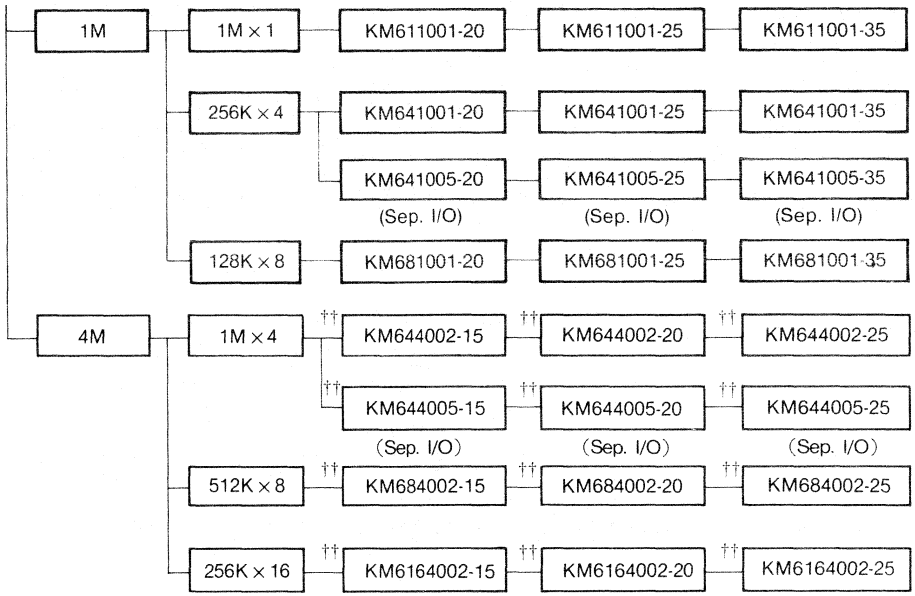
Pseudo SRAM Product Tree



* New Product
† Preliminary Product
†† Under Development

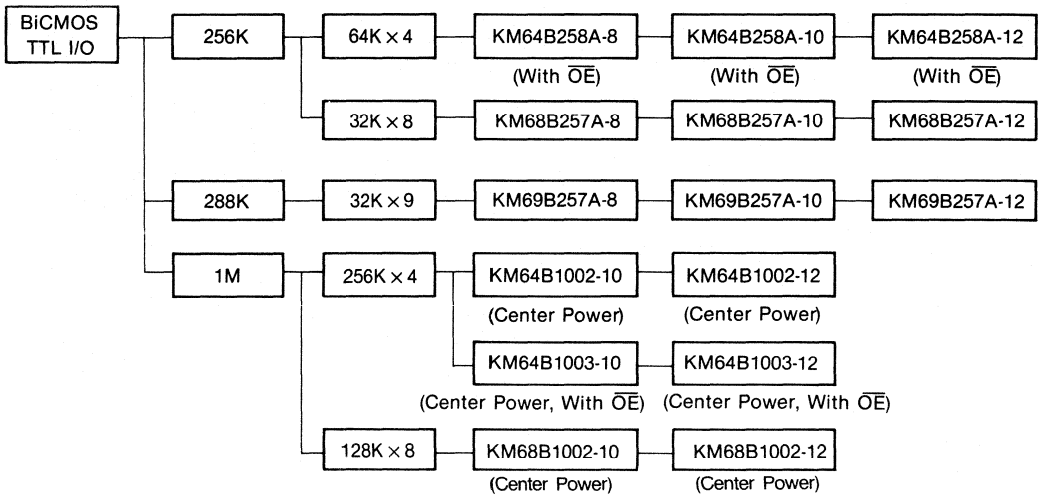
High Speed SRAM



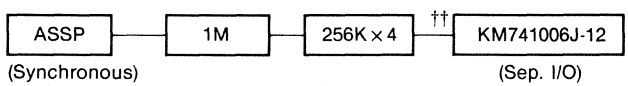

1M
1M × 1
KM611001-20
KM611001-25
KM611001-35
256K × 4
KM641001-20
KM641001-25
KM641001-35
KM641005-20
KM641005-25
KM641005-35
(Sep. I/O)
(Sep. I/O)
(Sep. I/O)
128K × 8
KM681001-20
KM681001-25
KM681001-35
4M
1M × 4
††
KM644002-15
KM644002-20
KM644002-25
KM644005-15
KM644005-20
KM644005-25
(Sep. I/O)
(Sep. I/O)
(Sep. I/O)
512K × 8
KM684002-15
KM684002-20
KM684002-25
256K × 16
KM6164002-15
KM6164002-20
KM6164002-25

1

*** BiCMOS SRAM**

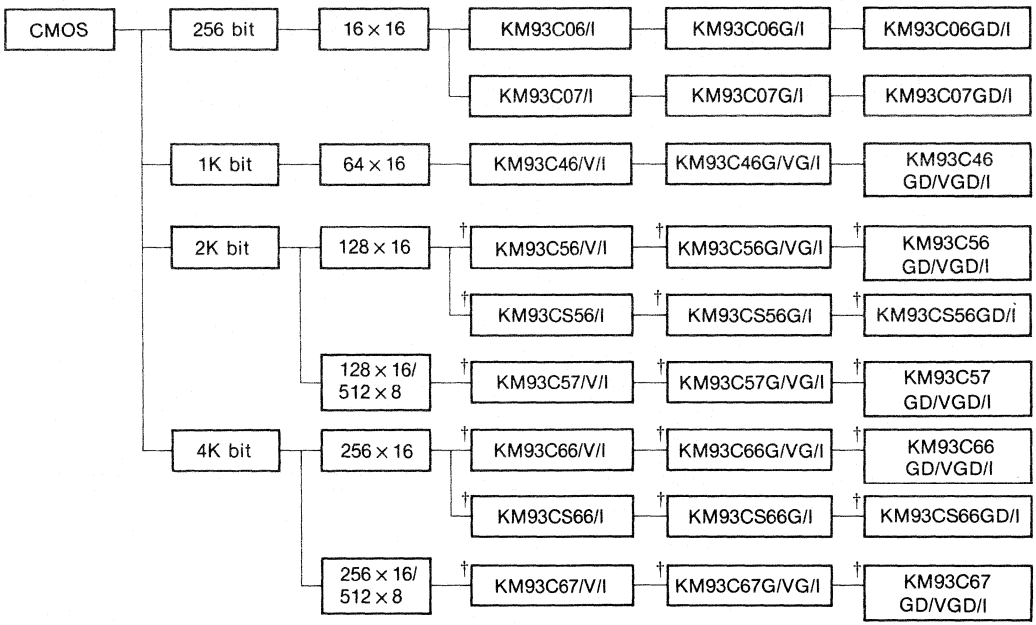


Specialty SRAM

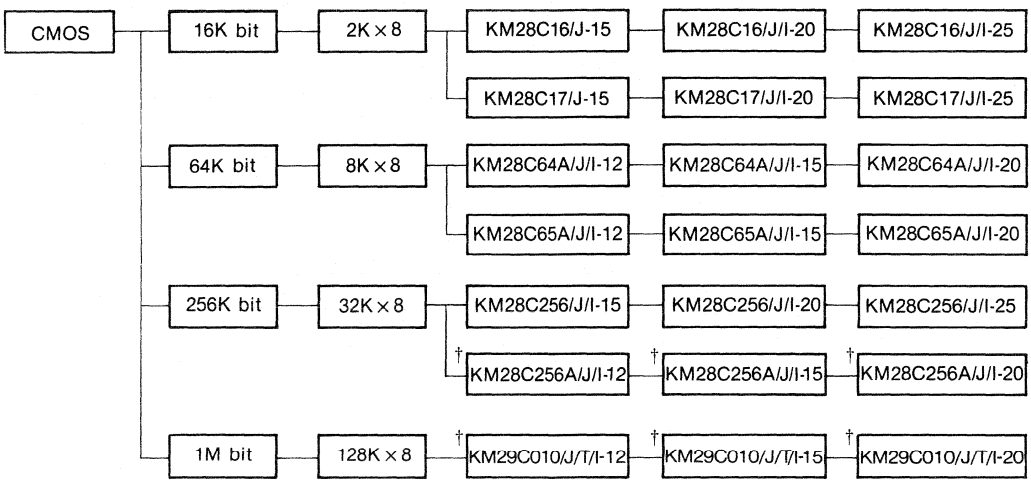


* New Product
† Preliminary Product
†† Under Development

1.5 Serial EEPROM

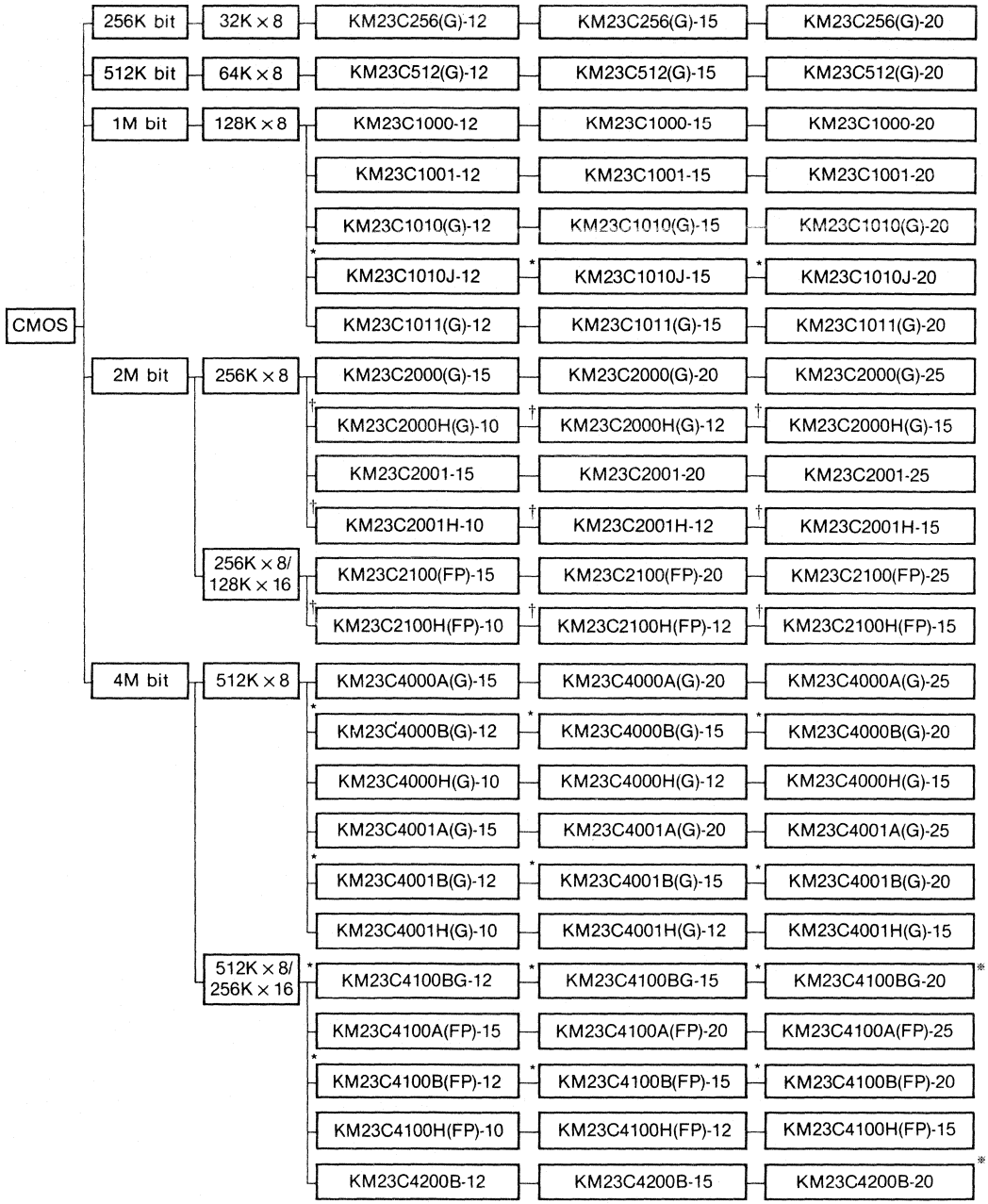


Parallel EEPROM



* New Product † Preliminary Product

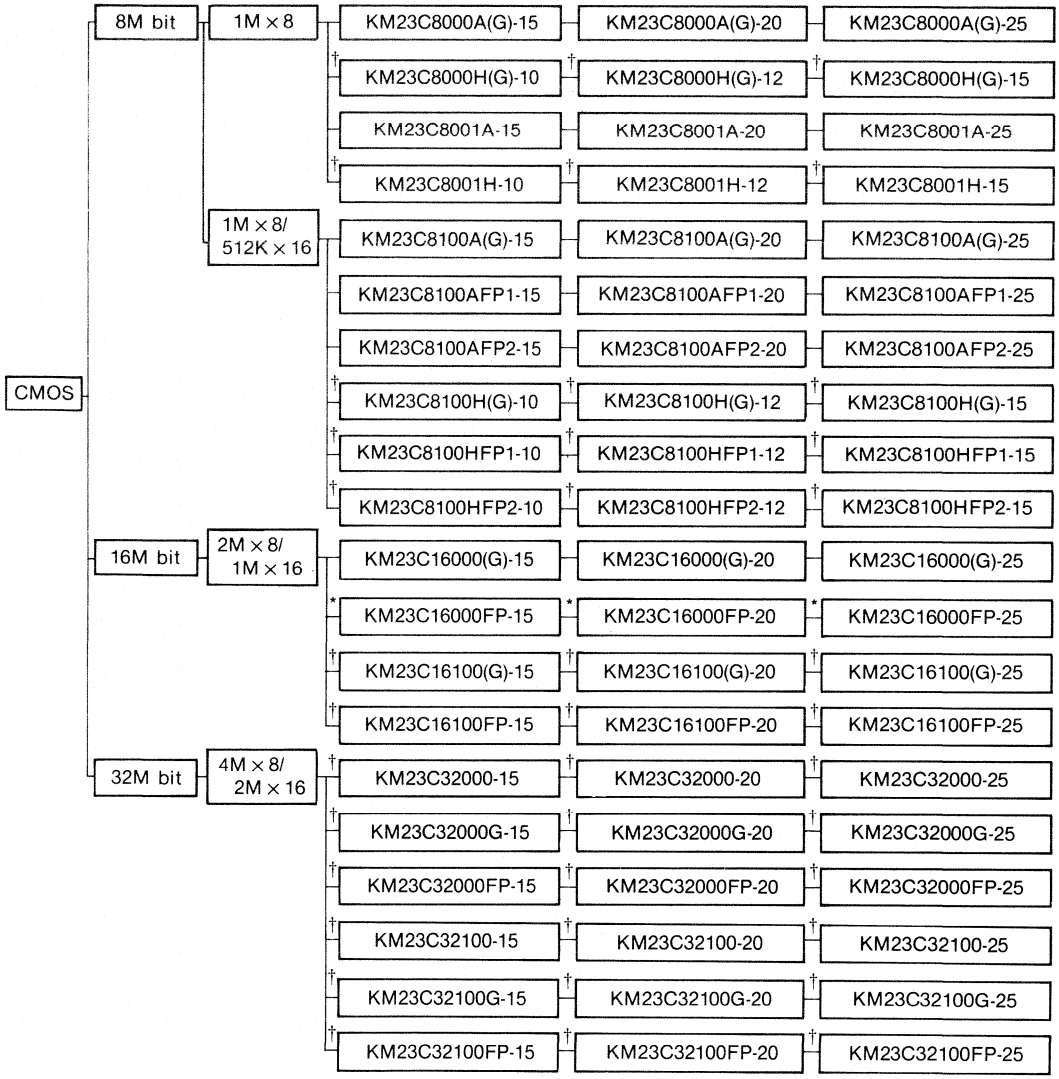
1.6 MASKROM- I (Low Density)



* New Product † Under Development

※ Both A and B ver. are available in 3Q '92

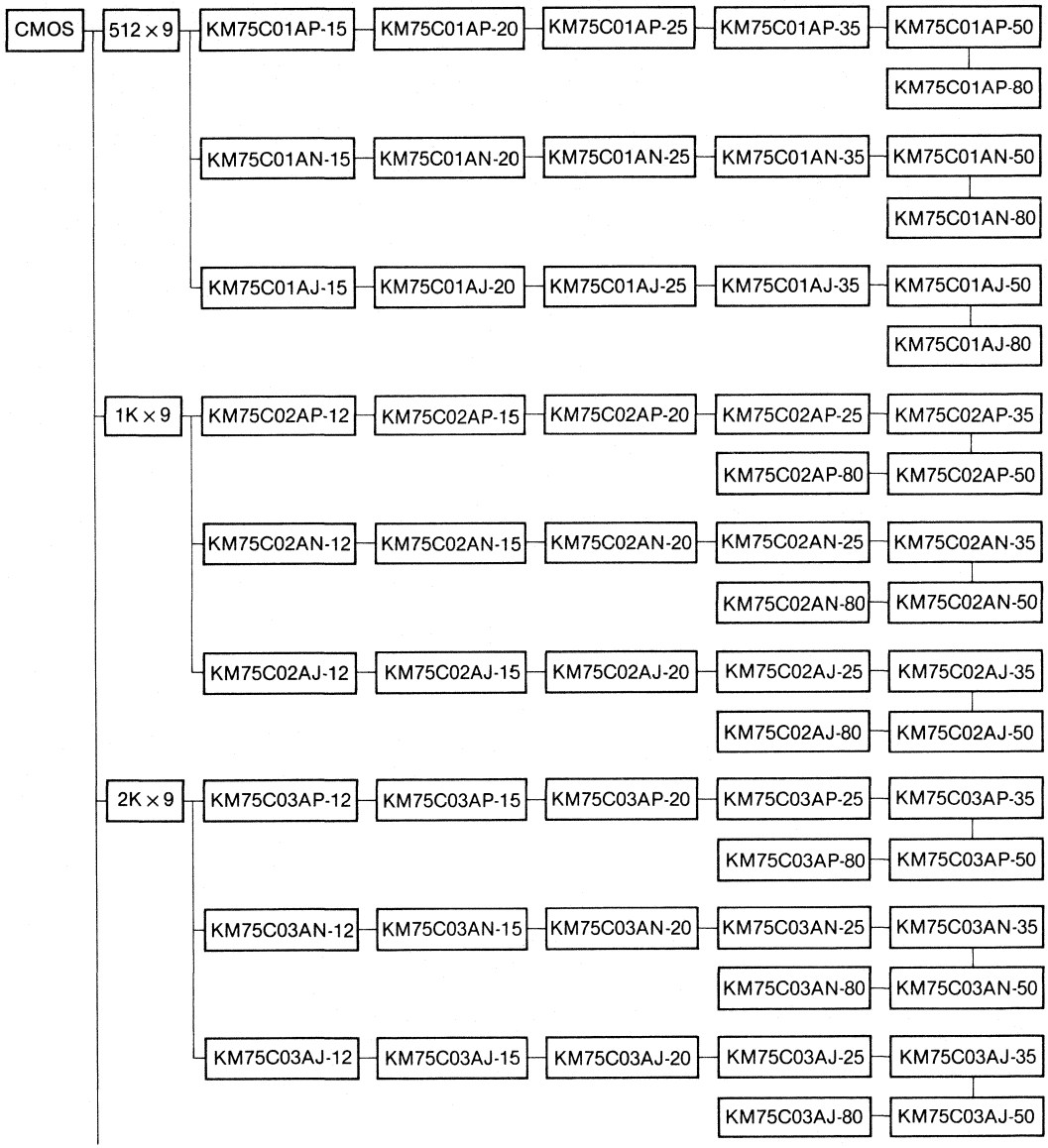
MASKROM-II (High Density)

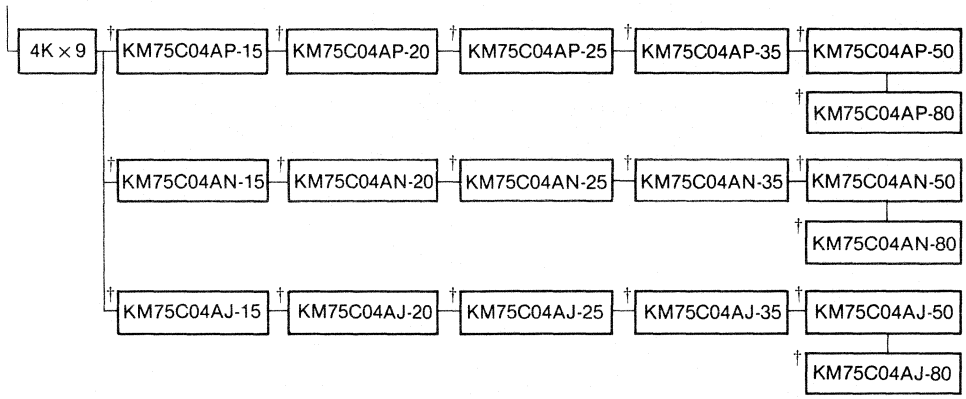


* New Product
† Under Development

1.7 Application Specific Memory

STANDARD FIFO





*AP: PDIP (0.6″)
AN: PDIP (0.3″)
AJ: PLCC
†: Preliminary Product

1

2. PRODUCT GUIDE

2.1 Dynamic RAM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
256K bit	KM41C256P	256K x 1	70/80/100	CMOS	Fast Page	16 Pin DIP	Now
	KM41C256J	256K x 1	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C256Z	256K x 1	70/80/100	CMOS	Fast Page	16 Pin ZIP	Now
	KM41C257P	256K x 1	70/80/100	CMOS	Nibble Mode	16 Pin DIP	Now
	KM41C257J	256K x 1	70/80/100	CMOS	Nibble Mode	18 Pin PLCC	Now
	KM41C257Z	256K x 1	70/80/100	CMOS	Nibble Mode	16 Pin ZIP	Now
	KM41C258P	256K x 1	70/80/100	CMOS	Static Column	16 Pin DIP	Now
	KM41C258J	256K x 1	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C258Z	256K x 1	70/80/100	CMOS	Static Column	16 Pin ZIP	Now
	KM41C464P	64K x 4	70/80/100	CMOS	Fast Page	18 Pin DIP	Now
	KM41C464J	64K x 4	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C464Z	64K x 4	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C466P	64K x 4	70/80/100	CMOS	Static Column	18 Pin DIP	Now
	KM41C466J	64K x 4	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C466Z	64K x 4	70/80/100	CMOS	Static Column	20 Pin ZIP	Now
1M bit	KM41C1000CP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CLP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CLJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CLZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CLV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CLVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CLT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CLTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CSLP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CSLJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CSLZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CSLV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CSLVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CSLT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CSLTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1001CP	1M x 1	60/70/80	CMOS	Nibble Mode	18 Pin DIP	Now
	KM41C1001CJ	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin SOJ	Now
	KM41C1001CZ	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin ZIP	Now
	KM41C1001CV	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Forward)	Now
	KM41C1001CVR	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Reverse)	Now
	KM41C1001CT	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Forward)	Now
	KM41C1001CTR	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Reverse)	Now
	KM41C1002CP	1M x 1	60/70/80	CMOS	Static Column	18 Pin DIP	Now
	KM41C1002CJ	1M x 1	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM41C1002CZ	1M x 1	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM41C1002CV	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM41C1002CVR	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM41C1002CT	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM41C1002CTR	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
1M bit	KM44C256CP	256K x 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CJ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CZ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CV	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CVR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CT	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CTR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CLP	256K x 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CLJ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CLZ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CLV	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CLVR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CLT	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CLTR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CSLP	256K x 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CSLJ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CSLZ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CSLV	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CSLVR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CSLT	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CSLTR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C266CP	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin DIP	Now
	KM44C266CJ	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin SOJ	Now
	KM44C266CZ	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin ZIP	Now
	KM44C266CV	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C266CVR	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C266CT	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C266CTR	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Reverse)	Now
	KM44C258CP	256K x 4	60/70/80	CMOS	Static Column	20 Pin DIP	Now
	KM44C258CJ	256K x 4	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM44C258CZ	256K x 4	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM44C258CV	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM44C258CVR	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM44C258CT	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM44C258CTR	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now
	KM44C268CP	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin DIP	Now
	KM44C268CJ	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin SOJ	Now
	KM44C268CZ	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin ZIP	Now
	KM44C268CV	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C268CVR	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C268CT	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C268CTR	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Reverse)	Now
4M bit	*KM41C4000BP	4M x 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	*KM41C4000BJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	*KM41C4000BLP	4M x 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M bit	*KM41C4000BLJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BLZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BLV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BLVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BLT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BLTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	*KM41C4000BSLP	4M x 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	*KM41C4000BSLJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BSLZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BSLV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BSLVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BSLT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BSLTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
4M B/W	*KM48C512J	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512Z	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512T	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512TR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512LJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512LZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512LT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512LTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512SLJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512SLZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512SLT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512SLTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512LLJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512LLZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512LLT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512LLTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512J	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512Z	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512T	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512TR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512LJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512LZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512LT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512LTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512SLJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512SLZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512SLT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512SLTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512LLJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512LLZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512LLT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512LLTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM416C256J	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256Z	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256LJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256LZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256SLJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256SLZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256LLJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256LLZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M B/W	*KM418C256J	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256Z	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256LJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256LZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256SLJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256SLZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256LLJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256LLZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
16M	*KM41C16000J	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16000T	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000TR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000LJ	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16000LT	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000LTR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100J	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16100T	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100TR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100LJ	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16100LT	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100LTR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000J	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4000T	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000TR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000LJ	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4000LT	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000LTR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100J	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4100T	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100TR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100LJ	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4100LT	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100LTR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
16M B/W	†KM48C2000J	2M x 8	60/70/80	CMOS	Fast Page	28 Pin SOJ	3Q, '92
	†KM48C2100J	2M x 8	60/70/80	CMOS	Fast Page	28 Pin SOJ	3Q, '92
	†KM416C1000J	1M x 16	70/80/100	CMOS	Fast Page	42 Pin SOJ	4Q, '92
	†KM416C1200J	1M x 16	70/80/100	CMOS	Fast Page	42 Pin SOJ	4Q, '92

*: New Product †: Preliminary Product

2.2 Dynamic RAM Module

Based Component	Part Number	Organization	Speed(ns)	Feature	Package	PCB height(In)	Remark
1M DRAM Base	KMM58256CN	256K x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM59256CN	256K x 9	70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM581000C	1M x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM591000C	1M x 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM536256C/CG	256K x 36	70/80	Fast Page	S, 72 Pin SIMM	1.0	Now
	KMM532512CV/CVG	512K x 32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM536512C/CG	512K x 36	70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM540512C/CG/CM	512K x 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
4M DRAM Base	KMM581000AN	1M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM581020AN	1M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM581000BN	1M x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	'92. 3Q
	KMM591000AN	1M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM591020AN	1M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM591000BN	1M x 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	'92. 3Q
	KMM584000A	4M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM584020A	4M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	*KMM584000B	4M x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	'92. 3Q
	KMM594000A	4M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM594020A	4M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	*KMM594000B	4M x 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	'92. 3Q
	KMM5321000AV/AVG	1M x 32	70/80/100	Fast Page	S, 72 Pin SIMM	0.855	Now
	*KMM5321000BV/BVG	1M x 32	60/70/80	Fast Page	S, 72 Pin SIMM	0.855	Now
	KMM5361000A/AG	1M x 36	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM5361000A1/A1G	1M x 36	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5361000B/BG	1M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	*KMM5361000B1/B1G	1M x 36	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	'92. 3Q
	KMM5322000AV/AVG	2M x 32	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5322000BV/BVG	2M x 32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	KMM5362000A/AG	2M x 36	70/80/100	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5362000A1/A1G	2M x 36	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5362000B/BG	2M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	'92. 3Q
	*KMM5362000B1/B1G	2M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	KMM5401000A/AG/AM	1M x 40	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5401000B/BG/BM	1M x 40	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	'92. 3Q
	KMM5402000A/AG/AM	2M x 40	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5402000B/BG/BM	2M x 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q

2.2 Dynamic RAM Module (Continued)

Based Component	Part Number	Organization	Speed(ns)	Feature	Package	PCB height(In)	Remark
4M B/W Wide DRAM Base	*KMM536256W/WG	256K × 36	70/80/100	Fast Page	S, 72 Pin SIMM	0.65	Now
	*KMM532512W3/W3G	512K × 32	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM536512W3/W3G	512K × 36	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
16M DRAM Base	*KMM584100N	4M × 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM594100N	4M × 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM5816000/T	16M × 8	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5816100/T	16M × 8	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5916000/T	16M × 9	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5916100/T	16M × 9	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5324100V/VG/VP	4M × 32	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5364100/G	4M × 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5364000H/HG	4M × 36	60/70/80	Fast Page	S, 72 Pin SIMM	1.25	Now
	*KMM5364100H/HG	4M × 36	60/70/80	Fast Page	S, 72 Pin SIMM	1.25	Now
	*KMM5328100V/VG/VP	8M × 32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5368100/G	8M × 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.375	Now
	*KMM5368000H/HG	8M × 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5368100H/HG	8M × 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5404000/G	4M × 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5404100/G	4M × 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
16M B/W Wide DRAM Base	††KMM5321000W/WG	1M × 32	70/80/100	Fast Page	S, 72 Pin SIMM	0.65	'92. 4Q
	††KMM5322000W/WG	2M × 32	70/80/100	Fast Page	D, 72 Pin SIMM	0.8	'92. 4Q

Note: S: Single Side, D: Double Side
*: New Product, ††: Under Development

2.3 Video RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
1M bit	KM424C256J	256K × 4	RAM: 80/100/120 SAM: 25/25/35	CMOS	Minimum Feature	28 Pin SOJ	Now
	KM424C256Z	256K × 4	RAM: 80/100/120 SAM: 25/25/35	CMOS	Minimum Feature	28 Pin ZIP	Now
	††KM424C257J	256K × 4	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	28 Pin SOJ 44 Pin TSOP II	3Q, '92
	††KM424C257Z	256K × 4	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	28 Pin ZIP	3Q, '92
	††KM428C128Z	128K × 8	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	40 Pin ZIP 44 Pin TSOP II	4Q, '91
	††KM428C128J	128K × 8	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	40 Pin SOJ	4Q, '91
256K bit	KM424C64P	64K × 4	RAM: 100/120 SAM: 25/35	CMOS	Minimum Feature	24 Pin DIP	Now
	KM424C64Z	64K × 4	RAM: 100/120 SAM: 25/35	CMOS	Minimum Feature	24 Pin ZIP	Now

2.4 Static RAM

Slow SRAM Function Guide

Capacity	Part Name	Organization	Speed	Technology	Power Dissipation			Package	Remark
					Active(max.) TTL. DC	Active(max.) TTL. Min	Standby(max.) CMOS		
64K	KM6264BL	8K x 8	70/100/120	CMOS	15mA	55mA	100μA	DIP/SDIP/SOP	Now
	KM6264BL-L	8K x 8	70/100/120	CMOS	15mA	55mA	10μA	DIP/SDIP/SOP	Now
256K	KM62256AL	32K x 8	80/100/120	CMOS	45mA	70mA	100μA	DIP/SOP	Now
	KM62256AL-L	32K x 8	80/100/120	CMOS	45mA	70mA	50μA	DIP/SOP	Now
	KM62256BL	32K x 8	70/85/100/120	CMOS	15mA	70mA	100μA	DIP/SDIP/SOP	Now
	KM62256BL-L	32K x 8	70/85/100/120	CMOS	15mA	70mA	20μA	DIP/SDIP/SOP	Now
	*KM62256BLI	32K x 8	70/100	CMOS	20mA	70mA	50μA	DIP/SOP	Now
	*KM62256BL-V	32K x 8	240	CMOS	15mA	70mA	50μA	DIP/SDIP/SOP	Now
512K	*KM68512L	64K x 8	55/70/85/100	CMOS	15mA	70mA	100μA	SOP/TSOP	Now
	*KM68512L-L	64K x 8	55/70/85/100	CMOS	15mA	70mA	20μA	SOP/TSOP	Now
1M	KM681000L	128K x 8	70/85/100/120	CMOS	25mA	70mA	100μA	DIP/SOP	Now
	KM681000L-L	128K x 8	70/85/100/120	CMOS	25mA	70mA	20μA	DIP/SOP	Now
	*KM681000AL	128K x 8	70/85/100/120	CMOS	15mA	70mA	100μA	DIP/SOP/TSOP	Now
	*KM681000AL-L	128K x 8	70/85/100/120	CMOS	15mA	70mA	20μA	DIP/SOP/TOP	Now
	*KM681000ALI	128K x 8	70/100	CMOS	20mA	70mA	100μA	DIP/SOP	Now
	*KM681000ALI-L	128K x 8	70/100	CMOS	20mA	70mA	50μA	DIP/SOP	Now
	*KM681000AL-V	128K x 8	240	CMOS	15mA	70mA	50μA	DIP/SOP/TSOP	Now
4M	†KM684000L	512K x 8	55/70/85/100	CMOS	25mA	70mA	100μA	DIP/SOP/TSOP	Now
	†KM684000L-L	512K x 8	55/70/85/100	CMOS	25mA	70mA	20μA	DIP/SOP/TSOP	Now

*: New Product †: Preliminary ††: Under Development

Pseudo SRAM Function Guide

Capacity	Part Name	Organization	Speed	Technology	Power Dissipation		Package	Remark
					Active(max.) TTL. Min	Standby(max.) CMOS		
1M	KM658128	128K x 8	80/100/120	CMOS	70mA	1mA	DIP/SDIP/SOP	Now
	KM658128L	128K x 8	80/100/120	CMOS	70mA	200μA	DIP/SDIP/SOP	Now
	KM658128L-L	128K x 8	80/100/120	CMOS	70mA	100μA	DIP/SDIP/SOP	Now
	KM658128LD	128K x 8	80/100/120	CMOS	70mA	200μA	DIP/SDIP/SOP	Now
	KM658128LD-L	128K x 8	80/100/120	CMOS	70mA	100μA	DIP/SDIP/SOP	Now
4M	*KM658128L	512K x 8	80/100/120	CMOS	75mA	200μA	DIP/SOP/TSOP	Now
	*KM658128L-L	512K x 8	80/100/120	CMOS	75mA	100μA	DIP/SOP/TSOP	Now

*: New Product †: Preliminary ††: Under Development

High Speed & Ultra High Speed SRAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
64K	KM6465A	16K × 4	25/35/45	CMOS	120	2	22SDIP	Now
	KM6465AL	16K × 4	25/35/45	CMOS	120	0.1	22SDIP	Now
	*KM6465B	16K × 4	12/15/20/25	CMOS	140	1	22SDIP	Now
	KM6465BL	16K × 4	12/15/20/25	CMOS	140	0.1	22DIP	Now
	KM6466A	16K × 4	25/35/45	CMOS	120	2	22SDIP/SOJ	Now
	KM6466AL	16K × 4	25/35/45	CMOS	120	0.1	22SDIP/SOJ	Now
	*KM6466B	16K × 4	12/15/20/25	CMOS	140	1	24SDIP/SOJ	Now
	KM6466BL	16K × 4	12/15/20/25	CMOS	140	0.1	24DIP/SOJ	Now
	*KM6865B	8K × 8	12/15/20/25	CMOS	140	1	28SDIP/SOJ	Now
	KM6865BL	8K × 8	12/15/20/25	CMOS	140	0.1	28DIP/SOJ	Now
256K	KM61257A	256K × 1	25/35/45	CMOS	100	2	24SDIP/SOJ	Now
	KM61257AL	256K × 1	25/35/45	CMOS	100	0.1	24SDIP/SOJ	Now
	KM64257A	64K × 4	25/35/45	CMOS	120	2	24SDIP/SOJ	Now
	KM64257AL	64K × 4	25/35/45	CMOS	120	0.1	24SDIP/SOJ	Now
	†KM64258B	64K × 4	15/20/25	CMOS	140	2	28SDIP/SOJ	Now
	†KM64B258A	64K × 4	8/10/12	BiCMOS	185	20	28SOJ	Now
	*KM64259B	64K × 4	15/20/25	CMOS	140	2	28SDIP/SOJ	Now
	*KM64260B	64K × 4	20/25	CMOS	140	2	28SDIP/SOJ	Now
	*KM68257B	32K × 8	15/20/25	CMOS	150	2	28SDIP/SOJ	Now
	*KM68257BL	32K × 8	15/20/25	CMOS	150	0.1	28SDIP/SOJ	Now
	†KM68B257A	32K × 8	8/10/12	BiCMOS	185	20	28SOJ	4Q '92
	KM69B257A	32K × 9	8/10/12	BiCMOS	185	20	28SOJ	4Q '92
512K	†KM616513	32K × 16	17/20/25	CMOS	180	2	40SOJ	2Q '93
1M	*KM611001	1M × 1	20/25/35	CMOS	130	2	28SDIP/SOJ	Now
	*KM641001	256K × 4	20/25/35	CMOS	150	2	28SDIP/SOJ	Now
	*KM641005	256K × 4	20/25/35	CMOS	150	2	32SDIP/SOJ	Now
	KM64B1002	256K × 4	10/12	BiCMOS	150	10	28SOJ	4Q '92
	KM64B1003	256K × 4	10/12	BiCMOS	150	10	32SOJ	4Q '92
	*KM681001	128K × 8	20/25/35	CMOS	170	2	32SDIP/SOJ	Now
	KM68B1002	512K × 8	10/12	BiCMOS	160	10	32SOJ	4Q '92

Synchronous SRAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
1M	†KM741006	256K × 4	12	CMOS	190	40	36SOJ	4Q '92

2.5 EEPROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remarks
256 bit	KM93C06/G/GD/I	16 x 16	1MHz	CMOS	Ext.-timed	8DIP/8SOP	Now
	KM93C07/G/GD/I	16 x 16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
1K bit	KM93C46/G/GD/I	64 x 16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
	KM93C46V/VG/VGD/I	64 x 16	250KHz	CMOS	3.0V Operation	8DIP/8SOP	Now
2K bit	KM93C56/G/GD/I	128 x 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	3Q '92
	KM93CS56/G/GD/I	128 x 16	1MHz	CMOS	Data Protect	8DIP/8SOP	3Q '92
	KM93C57/G/GD/I	256 x 8/128 x 16	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q '92
	KM93C56V/VG/VGD/I	128 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
	KM93C57V/VG/VGD/I	256 x 8/128 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
4K bit	KM93C66/G/GD/I	256 x 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	3Q '92
	KM93CS66/G/GD/I	256 x 16	1MHz	CMOS	Data Protect	8DIP/8SOP	3Q '92
	KM93C67/G/GD/I	512 x 8/128 x 16	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q '92
	KM93C66V/VG/VGD/1	256 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
	KM93C67V/VG/VGD/I	512 x 8/128 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
16K bit	KM28C16/J	2K x 8	150/200/250	CMOS	32B Page Mode, D-P	24DIP/32PLCC	Now
	KM28C16I/JI	2K x 8	200/250	CMOS	Industrial	24DIP/32PLCC	Now
	KM28C17/J	2K x 8	150/200/250	CMOS	32B Page Mode, D-P, R/B	28DIP/32PLCC	Now
	KM28C17I/JI	2K x 8	200/250	CMOS	Industrial	28DIP/32PLCC	Now
64K bit	KM28C64A/AJ	8K x 8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C64AI/AJI	8K x 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C65A/AJ	8K x 8	120/150/200	CMOS	64B Page Mode, D-P, R/B	28DIP/32PLCC	Now
	KM28C65AI/AJI	8K x 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
256K bit	KM28C256/J	32K x 8	150/200/250	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C256I/JI	32K x 8	150/200/250	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C256A/AJ	32K x 8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	4Q '92
	KM28C256AI/AJI	32K x 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	4Q '92
1M bit	KM29C010/J/T	128K x 8	120/150/200	CMOS	128B Page Mode, D-P, T-B	32DIP/32PLCC	4Q '92
	KM29C010I/JI	128K x 8	120/150/200	CMOS	Industrial	32TSOP	4Q '92

*: D-P: Data-Polling, R/B: Ready/Busy, T-B: Toggle Bit

2.6 Mask ROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
256K bit	KM23C256(G)	32K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
512K bit	KM23C512(G)	64K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
1M bit	KM23C1000	128K x 8	120/150/200	CMOS	Programmable CE	28DIP	Now
	KM23C1001	128K x 8	120/150/200	CMOS	Programmable OE	28DIP	Now
	KM23C1010(G)	128K x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	*KM23C1010J	128K x 8	120/150/200	CMOS	Programmable CE & OE	32PLCC	Now
	KM23C1011(G)	128K x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
2M bit	KM23C2000(G)	256K x 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	†KM23C2000H(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	3Q '92
	KM23C2001	256K x 8	150/200/250	CMOS	Programmable OE	32DIP	Now
	†KM23C2001H	256K x 8	100/120/150	CMOS	Programmable OE	32DIP	3Q '92
	KM23C2100(FP)	256K x 8/ 128K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	†KM23C2100H(FP)	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	3Q '92
4M bit	KM23C4000A(G)	512K x 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	*KM23C4000B(G)	512K x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C4000H(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C4001A(G)	512K x 8	150/200/250	CMOS	Programmable OE	32DIP(32SOP)	Now
	*KM23C4001B(G)	512K x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
	KM23C4001H(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	Now
	*KM23C4100BG	512K x 8/ 256K x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40SOP	Now
	KM23C4100A(FP)	512K x 8/ 256K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	†KM23C4100B(FP)	512K x 8/ 256K x x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	2Q '92
	KM23C4100H(FP)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	KM23C4200B	512K x 8/ 256K x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	Now

Mask ROM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
8M bit	KM23C8000A(G)	1M x 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	†KM23C8000H(G)	1M x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	3Q '92
	KM23C8001A	1M x 8	150/200/250	CMOS	Programmable OE	32DIP	Now
	†KM23C8001H	1M x 8	100/120/150	CMOS	Programmable OE	32DIP	3Q '92
	KM23C8100A(G)	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44SOP)	Now
	KM23C8100AFP1	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44QFP	Now
	KM23C8100AFP2	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	Now
	†KM23C8100H(G)	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44SOP)	3Q '92
	†KM23C8100HFP1	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	44QFP	3Q '92
	†KM23C8100HFP2	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	3Q '92
16M bit	KM23C16000(G)	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	Now
	*KM23C16000FP	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	Now
	†KM23C16100(G)	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	3Q '92
	†KM23C16100FP	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	3Q '92
32M bit	†KM23C32000	2M x 16	150/200/250	CMOS	Programmable CE & OE	42DIP	4Q '92
	†KM23C32000G	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	4Q '92
	†KM23C32000FP	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	4Q '92
	†KM23C32100	2M x 16	150/200/250	CMOS	Programmable CE & OE	42DIP	4Q '92
	†KM23C32100G	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	4Q '92
	†KM23C32100FP	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	4Q '92

*: New Product †: Under Development

2.7 FIFO

Capacity	Part Number	Organization	Speed	Technology	Features	Package	Remark
Standard FIFO	KM75C01AP	512 × 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	Now
	KM75C01AN	512 × 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	Now
	KM75C01AJ	512 × 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C02AP	1K × 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	Now
	KM75C02AN	1K × 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	Now
	KM75C02AJ	1K × 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C03AP	2K × 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	Now
	KM75C03AN	2K × 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	Now
	KM75C03AJ	2K × 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C04AP	4K × 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6″)	4Q '92
	KM75C04AN	4K × 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3″)	4Q '92
	KM75C04AJ	4K × 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	4Q '92

*: New Product
†: Preliminary Product

3. CROSS REFERENCE GUIDE

3.1 DRAM

Density	Org.	Mode	Samsung	Toshiba	Hitachi	Fujitsu	NEC	Oki
256K	×1	F. Page	KM41C256	TC51256	HM51256	MB81256	μPD41256	MSM51C256
		Nibble	KM41C257	TC51257	—	MB81257	—	MSM41257
		S. Column	KM41C258	TC51258	HM51258	MB81258	—	—
	×4	F. Page	KM41C464	TC51464	HM50464	MB81464	μPD41464	MSM41464
		S. Column	KM41C466	TC51466	—	MB81466	—	—
1M	×1	F. Page	KM41C1000	TC511000	HM511000	MB81C1000	μP0421000	MSM511000
		Nibble	KM41C1001	TC511001	HM511001	MB81C1001	μP0421001	MSM511001
		S. Column	KM41C1002	TC511002	HM511002	MB81C1002	μP0421002	MSM511002
	×4	F. Page	KM44C256	TC514256	HM514256	MB81C4256	μP0424256	MSM514256
		S. Column	KM44C258	TC514258	HM514258	MB81C4258	μP0424258	MSM514258
4M	×1	F. Page	KM41C4000	TC514100	HM514100	MB814100	μPD424100	MSM514100
		Nibble	KM41C4001	TC514101	HM514101	MB814101	μPD424101	MSM514101
		S. Column	KM41C4002	TC514102	HM514102	MB814102	μPD424102	MSM514102
	×4	F. Page	KM44C1000	TC514400	HM514400	MB814400	μPD424400	MSM514400
		S. Column	KM44C1002	TC514402	HM514402	MB814402	μPD424402	MSM514402
	×8	F. Page	KM48C512	TC514800A	HM514800	MB814800A	μPD424800	—
	×9	F. Page	KM49C512	TC514900A	HM514900	—	μPD424900	—
	×16	F. Page	KM416C256	TC514170B	HM514170	MB814170A	μPD424170	—
	×18	F. Page	KM418C256	TC514280B	HM514280	—	μPD424280	—
16M	×1	F. Page	KM41C16000	TC5116100	HM5116100	MB8116100	μPD4216100	—
	×4	F. Page	KM44C4000	TC5116400	HM5116400	MB8116400	μPD4216400	—

3.2 DYNAMIC RAM MODULE

Density	Organization	Samsung	Toshiba	Hitachi	NEC
2M bit	256K × 8(2C)	KMM58256CN	THM82500	HB56025608	—
2.3M bit	256K × 9(3C)	KMM59256CN	THM92500	HB56025609	—
8M bit	1M × 8	KMM581000	THM81000	HB56A18	MC-421000A8
9M bit	1M × 9	KMM591000	THM91000	HB56A19	MC-421000A9
8M bit	256K × 32	KMM532256	THM322500	HB56025632	—
9M bit	256K × 36	KMM536256	—	—	—
16M bit	512K × 32	KMM532512	THM325120	HB56051232	—
18M bit	512K × 36	KMM536512	—	HB56051236	—
20M bit	512K × 40	KMM540512	—	—	—
8M bit	1M × 8(2C)	KMM581000AN	—	HB56G18	—
9M bit	1M × 9(3C)	KMM591000AN	—	HB56G19	—
32M bit	4M × 8	KMM584000	THM84000	HB56A48	MC-424100A8
36M bit	4M × 9	KMM594000	THM94000	HB56A49	MC-424100A9
32M bit	1M × 32	KMM5321000	THM321000	HB56D132	—
36M bit	1M × 36	KMM5361000	THM5361020	HB56D136	MC-421000A36
64M bit	2M × 32	KMM5322000	THM322020	HB56D232	—
72M bit	2M × 36	KMM5362000	THM362020	HB56D236	MC-422000A36
40M bit	1M × 40	KMM5401000	THM401020	HB56A140	—
80M bit	2M × 40	KMM5402000	THM402020	—	—

3.3 VIDEO RAM

Density	Feature	Org.	Samsung	Toshiba	NEC	Hitachi	TI	Mitsubishi
256K	Minimum Feature	64K × 4	KM424C64		μPD41264 μPD42264	HM53461	TMS4461	M5M4C264
1M	Minimum Feature	256K × 4	KM424C256	TC524256 TC524256A/B	μPD42273	HM534251	TM544C250	
	Extended Feature	256K × 4	KM424C257	TC524258A/B TC524259B	μPD42274	HM534253 HM534252	TMS44C251	M5M442256
	Extended Feature	128K × 8	KM428C128	TC528126A/B TC528128A/B	μPD42275	HM538121 HM538122 HM538123	TMS48C121	M5M482128

3.4 Static RAM

Slow SRAM Cross Reference

Density	Org.	SAMSUNG	HITACHI	SONY	TOSHIBA	MITSUBISHI	NEC
64K	8K × 8	KM6264BL/BL-L	HM6264AL/AL-L	CXK5864BL	TC5565AL	M5M5165	μPD4364L/L-L
256K	32K × 8	KM62256AL/AL-L KM62256BL/BL-L	HM62256L/L-L	CXK58257L/L-L	TC55257L	M5M5265	μPD43256AL
512K	64K × 8	KM68512L/L-L	—	—	—	—	—
1M	128K × 8	KM681000L/L-L KM681000AL/AL-L	HM628128L/L-L	CXK581000L CXK581001L	TC551001L	M5M51000	μPD431000L
4M	512K × 8	KM684000L/L-L	HM628512	CXK584000L	TC554001L	M5M5408	μPD434000

Pseudo SRAM Cross Reference

Density	Org.	SAMSUNG	HITACHI	TOSHIBA	NEC	OKI	MOTOROLA
1M	128K × 8	KM658128/L/L-L	HM658128	TC518128A	μPD428128	MSM548128	MCM518128
4M	512K × 8	KM658512L/L-L	HM658512	TC518512	μPD428512	MSM548512	—

Fast SRAM

Density	Organization	Samsung	Hitachi	Cypress	Fujitsu	Micron	IDT	Motorola	Toshiba	Sony
64K	16K x 4	KM6465A/AL KM6465B/BL	HM6288/L	CY7C164 CY7C164A	MB81C74	MT5C6404	IDT7188	MCM6288	TC55416	CXK5464
	16K x 4 (With $\overline{OE}$)	KM6466A/AL KM6466B/BL	HM6289/L	CY7C166 CY7C166A	MB81C75	MT5C6405	IDT7189	MCM6290	TC55417	CXK5465
	8K x 8	KM6865B/BL		CY7C186A	MB81C78	MT5C6308	IDT7164	MCM6264	TC5588	CXK5863
256K	256K x 1	KM61257A/AL	HM6207H/L	CY7C197	MB81C81A	MT5C2561	IDT71257	MCM6207		CXK51256
	64K x 4	KM64257A/AL	HM6208H/L	CY7C194	MB81C84	MT5C2564	IDT71258	MCM6208	TC55464	CXK54256
	64K x 4 (With $\overline{OE}$)	KM64258B		CY7C196		MT5C2565	IDT61298	MCM6209	TC55465	
	64K x 4 (Sep. I/O, H-Z)	KM64259B		CY7C191	MB81C86		IDT71282			
	64K x 4 (Sep. I/O, L-Z)	KM64260B		CY7C192			IDT71281			
	32K x 8	KM68257B/BL	HM63832UH/L	CY7C199		MT5C2568	IDT71256	MCM6206	TC55328	CXK58258B
512K	32K x 16	KM616513							TC551632	
1M	1M x 1	KM611001	HM61100A/L	CY7C107		MT5C1001	IDT71027			
	256K x 4	KM641001	HM624256A/L	CY7C106		MT5C1005	IDT71028	MCM6229W		
	256K x 4 (Sep. I/O)	KM641005	HM624257A/L	CY7C101						CXK541000
	128K x 8	KM681001		CY7C108		MT5C1008	IDT71024	MCM6226W		CXK581020

BiCMOS SRAM

Density	Organization	Samsung	Hitachi	Cypress	Toshiba	Fijitsu	IDT	Motorola
256K	64K x 4(With OE)	KM64B258A	HM6709A	CY7B195	TC55B465		IDT61B298	MCM6709/A
	32K x 8	KM68B257A	HM628325H	CY7B199	TC55B328		IDT71B256	MCM6706/A
288K	32K x 9	KM69B257A			TC55B329			
1M	256K x 4 (Center Power)	KM64B1002			TC55B4256			MCM6728
	256K x 4 (Center Power, with OE)	KM64B1003			TC55B4257			MCM6729
	128K x 8 (Center Power)	KM68B1002			TC55B8128			MCM6726

3.5 EEPROM

Serial I/O EEPROM

Density	Samsung	N.S.	Exar	Micro Chip	SGSThomson	Catalyst	Rohm	AsahiKasai
256	KM93C06	NM9306		93C46	ST93C06			AK93C06
	KM93C07	NM9307		ER59256				
1K	KM93C46	NM9346	XRM93C46A	93C46	ST93C46T	CAT93C46A	BR93C46	AK93C46
	KM93CS46	NM93CS46			ST93C46		BR93CS46	
	KM93C46V	NM93C46L						
2K	KM93C56	NM93C56	XRM93C56A				BR93C56A	AK93C57
	KM93C57			93C56	ST93C56	CAT36C102		
	KM93CS56	NM93CS56			ST93CS56			
	KM93C56V	NM93C56L					BR93C56B	
	KM93C57V							
4K	KM93C66	NM93C66	XRM93C66B				BR93C66A	AK93C67
	KM93C67			93C66		CAT35C104		
	KM93CS66	NM93CS66			ST93CS66			
	KM93C66V	NM93C66L					BR93C66B	
	KM93C67V					CAT33T104		

Parallel EEPROM

Density	Samsung	Xicor	Seeq	Exel	Atmel	Hitachi	Oki	Catalyst
16K	KM28C16	X2816B X2816C	DQ2816A DQ5516A	XL2816A	AT28C16		MSM28C16A	CAT28C16A
	KM28C17		DQ2817A DQ5517A	XL2817A	AT28C17			CAT28C17A
64K	KM28C64A	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65A		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
256K	KM28C256	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256
	KM28C256A	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256
1M	KM29C010				AT29C010			

3.6 Mask ROM Cross Reference Guide-1

Density	Package	Org.	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
256K	28 DIP	x 8	KM23C256		HN623257P HN623257PZ HN623258P		LH23255D LH53259D	M5M23256P	MB83256	
	32 SOP	x 8	KM23C256G							
512K	28 DIP	x 8	KM23C512			TC53512CP	LH23512D LH53514D LH53515D		MB83512	
	32 DIP	x 8	KM23C512G							
1M	28 DIP	x 8	KM23C1000	μPD23C1000A	HN62321P HN62321BP HN62331P	TC531000CP	LH231000BD LH531000AD	M5M23C100 M5M231000	MB831000 MB831124	
			KM23C1001	μPD23C1010A	HN62321EP HN62331EP			M5M231001		
	32 DIP	x 8	KM23C1010	μPD23C1001E μPD23C1000EA	HN62321AP HN62331AP	TC531001CP	LH231100BD LH530800D LH530900D			
			KM23C1011							
	32 SOP	x 8	KM23C1010G		HN62321AF HN62331AF	TC531001CF				
			KM23C1011G							
2M	32 DIP	x 8	KM23C2000	μPD23C2001			LH532300D LH532100BD LH532200BD LH532400D		MB832000 MB832001	CXK382001
			KM23C2001							
	32 SOP	x 8	KM23C2000G							
	40 DIP	x 8/ x 16	KM23C2100	μPD23C2000 μPD23C2000A	HN62412P HN62422P		LH532000BD LH532500D			
	44 QFP	x 8/ x 16	KM23C2100FP		HN62412FP HN62422FP					

Mask ROM Cross Reference Guide—II

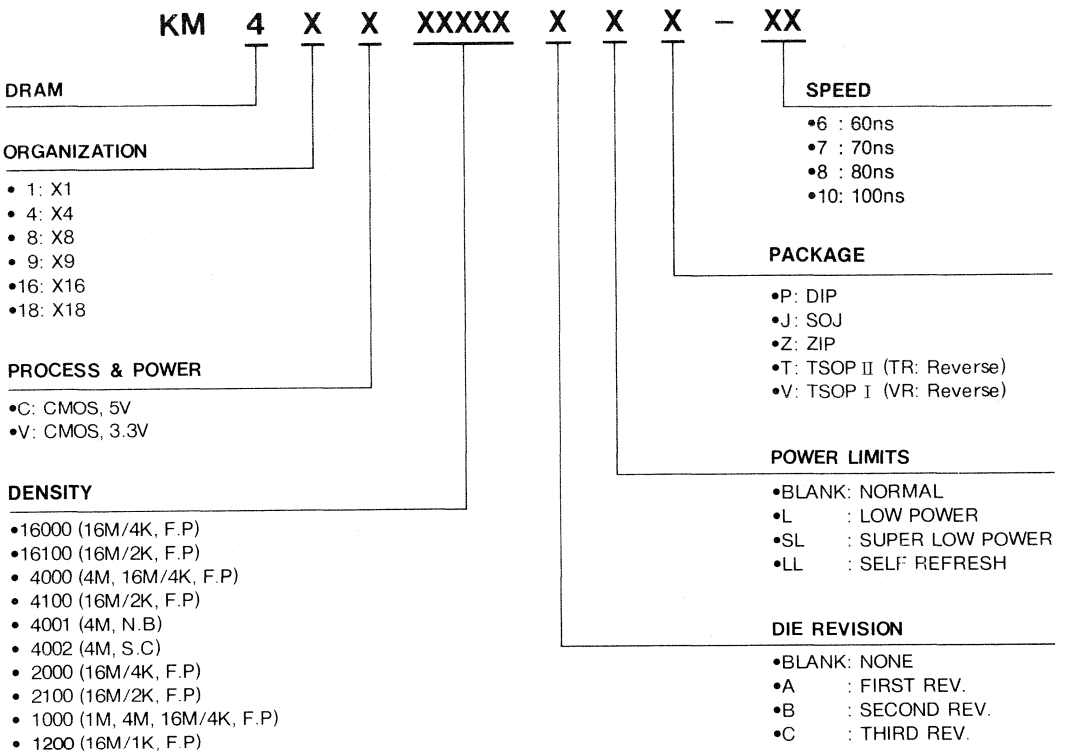
Density	Package	Org.	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
4M	32 DIP	x8	KM23C4000A	μPD23C4001E	HN62304BP	TC534000P	LH534100BD	M5M23C401AP	MB834000A	CXK384001
					HN62314BP	TC534000AP				
					HN62324BP					
					HN62344BP					
			KM23C4001A				LH534200BD			
							LH534300D			
							LH534400D			
	32 SOP	x8	KM23C4000AG	μPD23C4001E	HN62304BF	TC534000F	LH534100BN	M5M23401AFP		
					HN62314BF	TC534000AF				
					HN62324BF					
					HN62344BF					
			KM23C4001HG				LH534200BN			
	40 DIP	X8/x16	KM23C4100A	μPD23C4000	HN62404P	TC534200P	LH534000BD	M5M23C400AP	MB834100A	
				μPD23C4000A	HN62414P		LH534500D		MB834200A	
					HN62424P					
					HN62444P					
	40 SOP	x8/x16	KM23C4100BG			TC534200F				
	44 QFP	x8/x16	KM23C4100AFP		HN62404FP				MB834200A	
					HN62414FP					
					HN62424FP					
					HN62444FP					
8M	32 DIP	x8	KM23C8000A	μPD23C8001E	HN62308BP		LH538100D	M5M23801P	MB838000	CXK388000
			KM23C8001A				LH538200D			
	32 SOP	x8	KM23C8000AG		HN62308BF			M5M23801FP		
	42 DIP	x8/x16	KM23C8100A	μPD23C8000	HN62408P	TC538200P	LH538000D	M5M23800P	MB838200	
	44 SOP	x8/x16	KM23C8100AG			TC538200F	LH538000N	M5M23800FP		
	44 QFP	x8/x16	KM23C8100AFP1		HN62408FP					
	64 QFP	x8/x16	KM23C8100AFP2				LH538000M		MB838200	
16M	42 DIP	x8/x16	KM23C16000	μPD23C16000	HN624016P	TC5316200P		M5M23160P	MB831620P	
					HN624017P					
			KM23C16100					M5M23168P		
	44 SOP	x8/x16	KM23C16000G		HN624017FB	TC5316200F		M5M23160FP	MB831620PF	
			KM23C16100G					M5M23168FP		
	64 QFP	x8/x16	KM23C16000FP				LH5316000M			
			KM23C16100FP							
32M	42 DIP	x16	KM23C32000							
	44 SOP	x8/x16	KM23C32000G				LH5332000N			
	64 QFP	x8/x16	KM23C32000FP				LH5332000M			

3.7 FIFO

Capacity	Org.	Samsung	AMD	IDT	Sharp	Cypress	TI
Standard FIFO	512 x 9	KM75C01A	Am7201	IDT7201SA/LA	LH5496/D	CY7C420(1)	74ACT7201A
	1K x 9	KM75C02A	Am7202	IDT7202SA/LA	LH5497/D	CY7C424(5)	74ACT7202
	2K x 9	KM75C03A	Am7203	IDT7203S/L	LH5498/DKM7	CY7C428(9)	
	4K x 9	KM75C04A	Am7204	IDT7204S/L	LH5499/D		

4. ORDERING INFORMATION

4.1 DRAM



4.2 DRAM MODULE

MODULE PART NUMBERING SYSTEM

KM M W WW XXXX Y Y Y Y Y Y —ZZ

MEMORY

MODULE

PIN/EDGE CONNECTOR

- •5: DRAM SIMM (EDGE CONNECTOR)
- •4: DRAM SIP (PINS)

ORGANIZATION

- •8 : X8 bits wide
- •9 : X9 bits wide
- •18 : X18 bits wide
- •32 : X32 bits wide
- •33 : X33 bits wide
- •36 : X36 bits wide
- •40 : X40 bits wide
- •144: X144 bits wide

DENSITY & MODE/FEATURE

- 16000: 16M F. Page, 4K refresh
- 16100: 16M F. Page, 2K refresh
- 8000: 8M F. Page, 4K refresh
- 8100: 8M F. Page, 2K refresh
- 4000: 4M F. Page, 1K/4K refresh
- 4001: 4M Nibble
- 4002: 4M S. Column
- 4020: 4M F. Page (Low Power)
- 4040: 4M F. Page (S. Low Power)
- 4100: 4M F. Page, 1K/2K refresh
- 1000: 1M F. Page
- 1001: 1M Nibble
- 1002: 1M S. Column
- 1010: 1M F. Page, L. Profile (.505")
- 1020: 1M F. Page (Low Power)
- 1040: 1M F. Page (S. Low Power)
- 1005: 1M Slugger Module
- 512: 512K Page
- 514: 512K S. Column
- 532: 512K Page (Low Power)
- 256: 256K Page
- 258: 256K S. Column
- 276: 256K Page (Low Power)

SPEED

- •5 : 50ns
- •6 : 60ns
- •7 : 70ns
- •8 : 80ns
- •10: 100ns

LEAD FINISH/SPEC CUSTOMER

—STD. MODULE
- •BLANK: SOLDER
- •G : GOLD

—CUSTOMER
- •D: DEC
- •P: APPLE
- •H: HP
- •Q: COMPAQ
- •M: IBM

x 32 & x 33 ONLY PCB

- •V: x32 & x33 ONLY

NUMBER OF COMPONENTS

- •BLANK: MORE THAN 7 CHIPS
- •N : LESS THAN 8 CHIPS
- •W : BYTE-WORD WIDE BASE

PACKAGE (PCB) REVISION

- •BLANK: NONE
- •1 : FIRST REV.
- •2: SECOND REV.

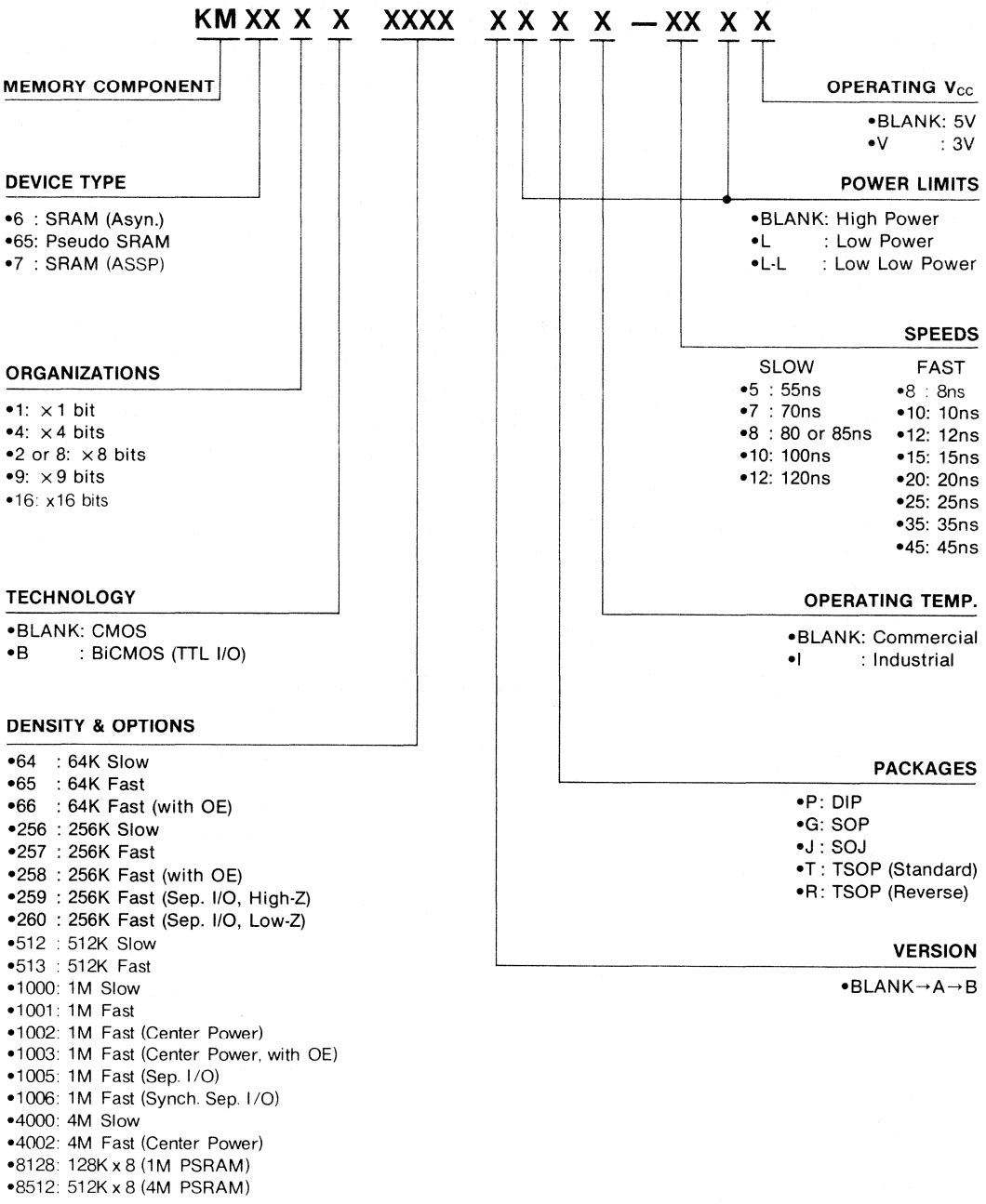
PACKAGE (COMPONENT) TYPE

- •BLANK: SOJ OR PLCC
- •*T : TSOP

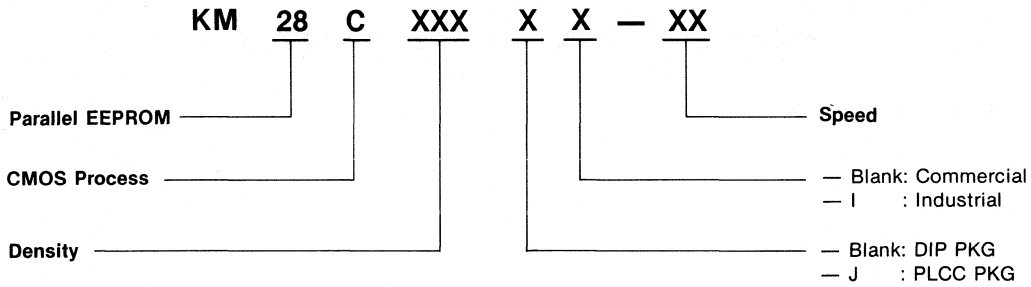
DIE (COMPONENT) REVISION

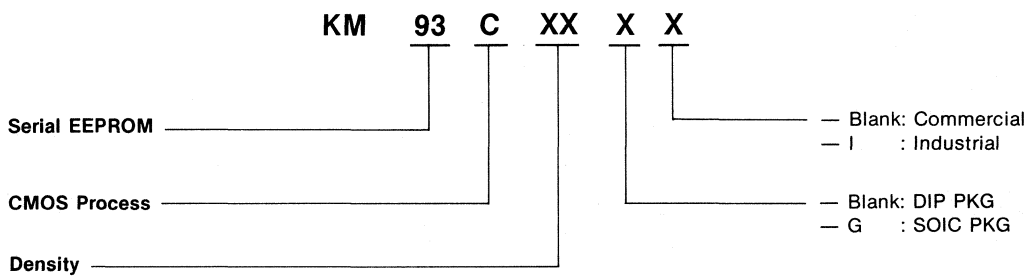
- •BLANK: NONE
- •A : FIRST REV.
- •B : SECOND REV.
- •C : THIRD REV.

4.3 SRAM ORDERING INFORMATION

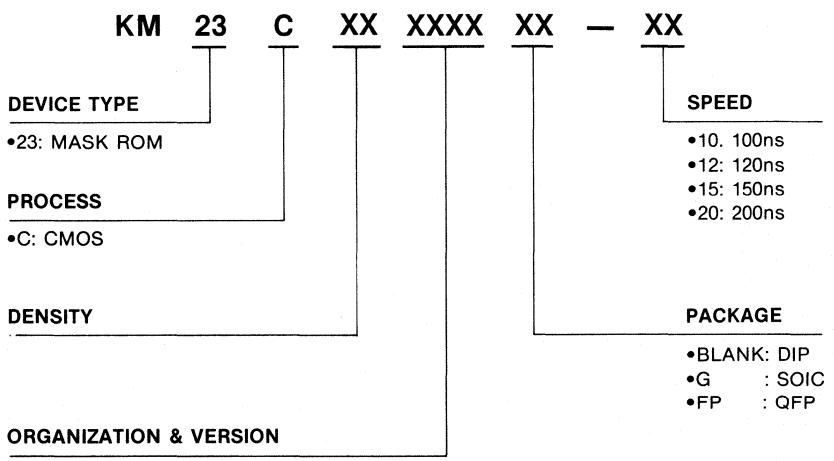


4.4 EEPROM

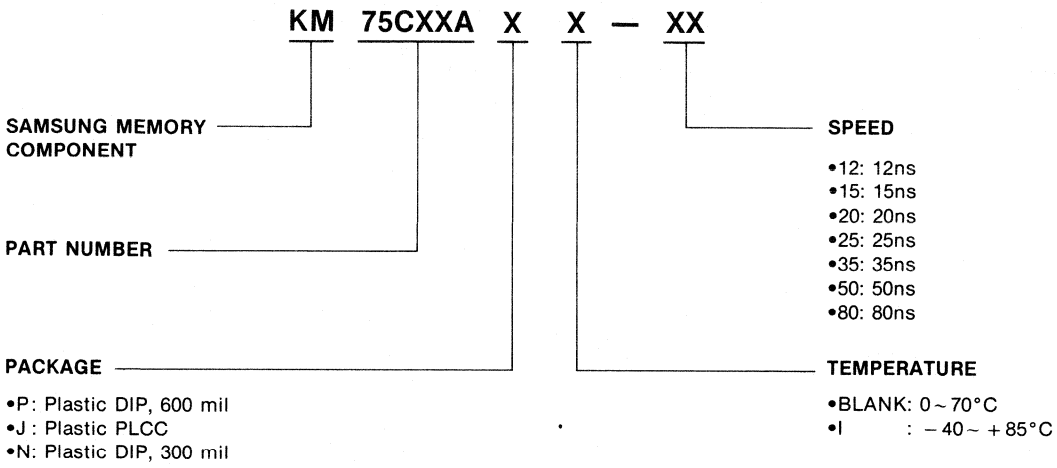




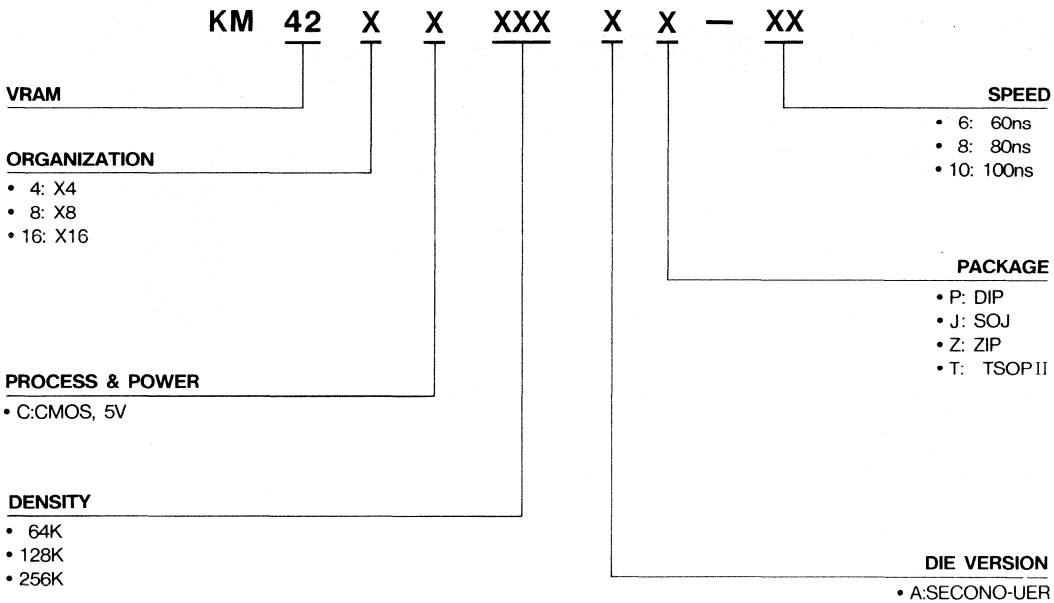
4.5 MASK ROM

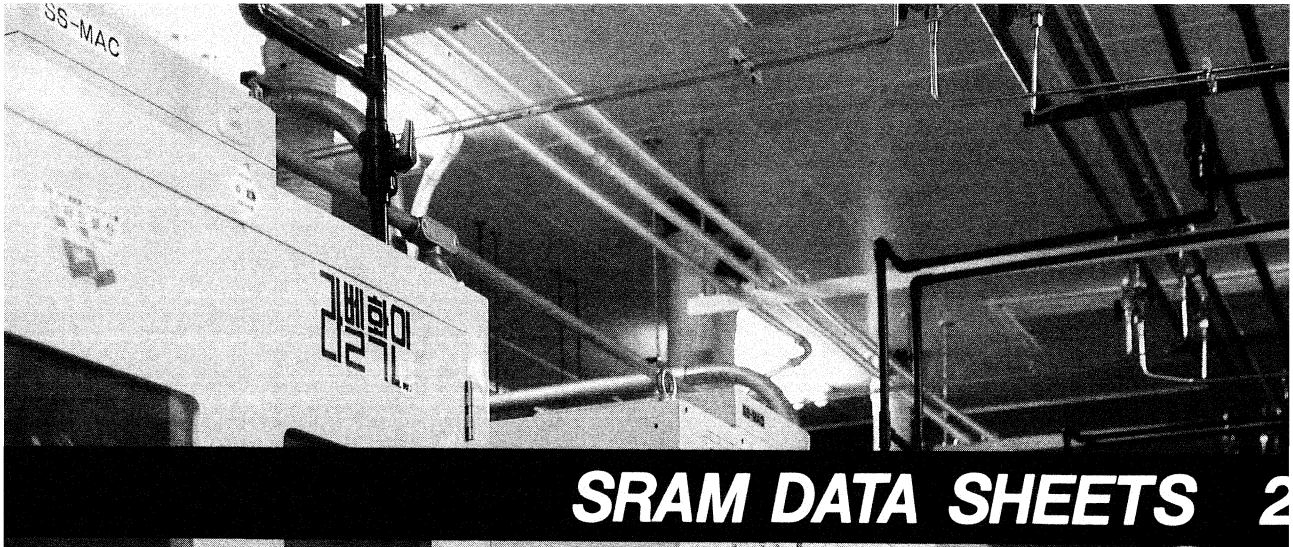


4.6 FIFO


KM 75CXXA X X — XX
SAMSUNG MEMORY COMPONENT
PART NUMBER
PACKAGE
•P: Plastic DIP, 600 mil
•J : Plastic PLCC
•N: Plastic DIP, 300 mil
SPEED
•12: 12ns
•15: 15ns
•20: 20ns
•25: 25ns
•35: 35ns
•50: 50ns
•80: 80ns
TEMPERATURE
•BLANK: 0 ~ 70°C
•I : −40 ~ +85°C

4.7 VRAM


KM 42 X X XXX X X — XX
VRAM
ORGANIZATION
• 4: X4
• 8: X8
• 16: X16
PROCESS & POWER
• C:CMOS, 5V
DENSITY
• 64K
• 128K
• 256K
SPEED
• 6: 60ns
• 8: 80ns
• 10: 100ns
PACKAGE
• P: DIP
• J: SOJ
• Z: ZIP
• T: TSOP II
DIE VERSION
• A:SECONO-UER



SRAM DATA SHEETS 2

Low Power Dissipation SRAMs

1. KM6264BL/BL-L
2. KM62256A/AL/AL-L
3. KM62256BL/BL-L
4. KM62256BLPI/BLGI
5. KM62256BL-V
6. KM68512L/L-L
7. KM681000L/L-L
8. KM681000AL/AL-L
9. KM681000ALI/ALI-L
10. KM681000AL-V
11. KM684000L/L-L

Pseudo SRAM

12. KM658128/L/L-L/LD/LD-L
13. KM658512L/L-L

High Speed SRAMs

14. KM6465A/AL
15. KM6465B/BL
16. KM6466A/AL
17. KM6466B/BL
18. KM6865B/BL
19. KM61257A/AL
20. KM64257A/AL
21. KM64258B
22. KM64B258A
23. KM64259B/KM64260B
24. KM68257B
25. KM68257BL
26. KM68B257A
27. KM69B257A
28. KM616513
29. KM611001
30. KM641001
31. KM64B1002
32. KM64B1003
33. KM641005
34. KM681001
35. KM68B1002
36. KM644002
37. KM644005
38. KM684002
39. KM6164002

Synchronous Static RAM

40. KM741006J

8K x 8 Bit Static RAM

FEATURES

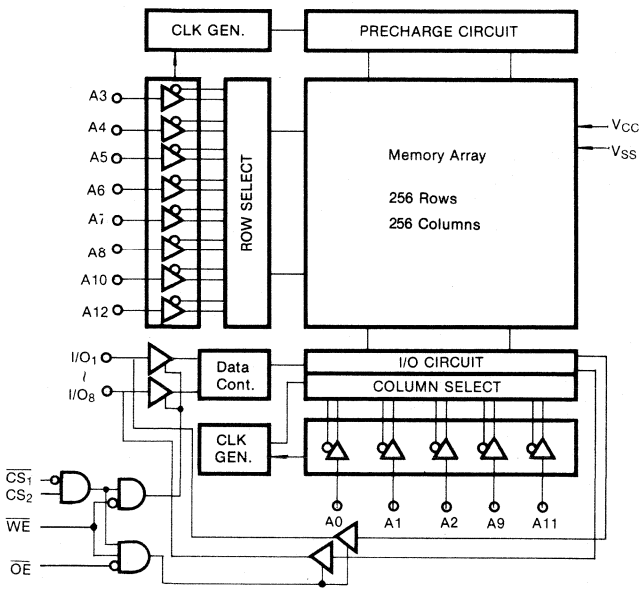
- **Fast Access Time: 70,100,120 ns (max.)**
- **Low Power Dissipation**
  Standby (CMOS): 10μW (typ.) L-Version
  5μW (typ.) LL-Version
  Operating: 55mW/MHz (max.)
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  —No clock or refresh required
- **Three State Output**
- **Low Data Retention Voltage: 2V (min.)**
- **JEDEC Standard pin Configuration**
  KM6264B/BL/BL-L: 28-pin DIP (600 mil)
  KM6264BS/BLS/BLS-L: 28-pin DIP (300 mil)
  KM6264BG/BLG/BLG-L: 28-pin SOP (330 mil)

GENERAL DESCRIPTION

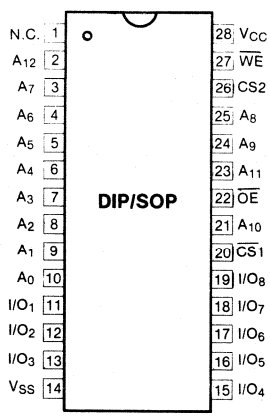
The KM6264B/BL/BL-L is a 65,536-bit high-speed Static Random Access Memory organized as 8,192 words by 8 bit.
The device is fabricated using Samsung's advanced CMOS process.
The KM6264B/BL/BL-L has an output enable input for precise control of the data outputs.
It also has chip select inputs for the minimum current power down mode.
The KM6264B/BL/BL-L has been designed for high speed and low power applications.
It is particularly well suited for battery back-up non-volatile memory applications.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$1, CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified.)

Item	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		−2		2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		−2		2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0mA				15	mA
Average Operating Current	I_{CC1}	Cycle time=1μs, 100% Duty $\overline{CS1}$≤0.2V, CS2≥V_{CC}−0.2V V_{IL}≤0.2V, V_{IH}≥V_{CC}−0.2V $I_{I/O}$=0mA				10	mA
	I_{CC2}	Min Cycle, 100% Duty	70ns			55	mA
		I_{OUT}=0mA	100/120ns			45	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}			0.2	2	mA
	I_{SB1}	$\overline{CS1}$≥V_{CC}−0.2V, CS2≤0.2V or CS2≥V_{CC}−0.2V	L		2	100	μA
			LL		1	10	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1mA		2.4			V

* Typ: V_{CC}=5V, T_A=25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

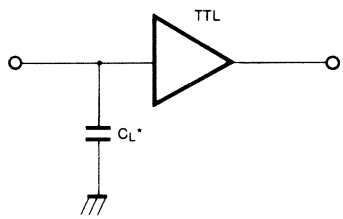
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS ($Ta = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 100$ pF + 1 TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6264BL-7 KM6264BL-7L		KM6264BL-10 KM6264BL-10L		KM6264BL-12 KM6264BL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		120		ns
Address Access Time	t_{AA}		70		100		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		100		120	ns
Output Enable to Valid Output	t_{OE}		35		50		60	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

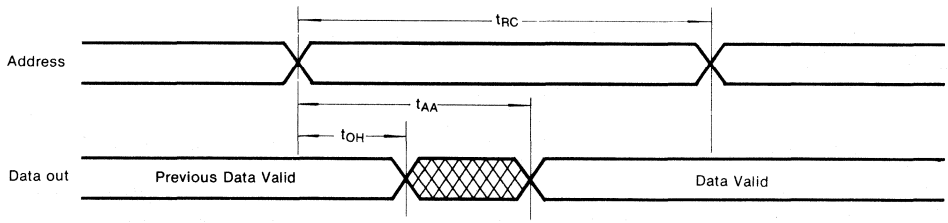
WRITE CYCLE

Parameter	Symbol	KM6264BL-7 KM6264BL-7L		KM6264BL-10 KM6264BL-10L		KM6264BL-12 KM6264BL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		120		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Write Pulse Width	t_{WP}	40		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		10		ns

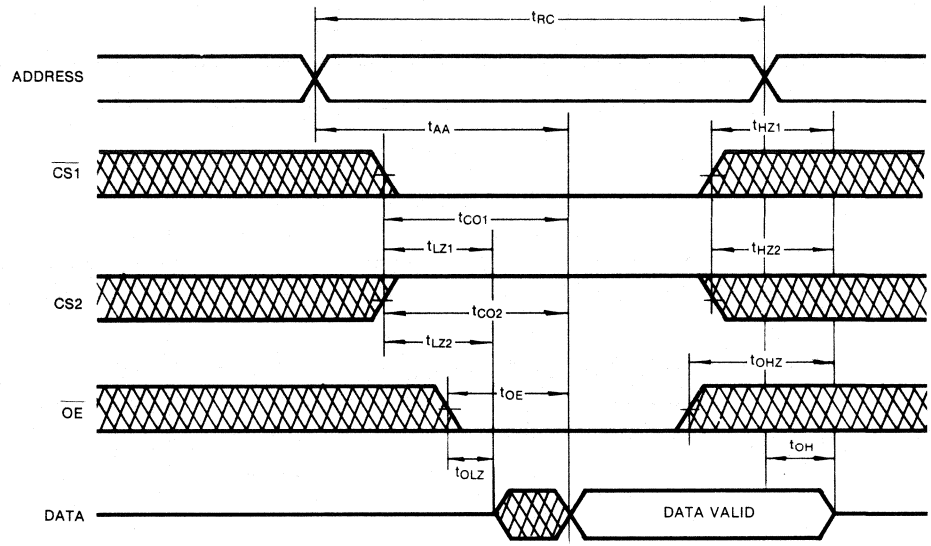
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO. 1

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$)



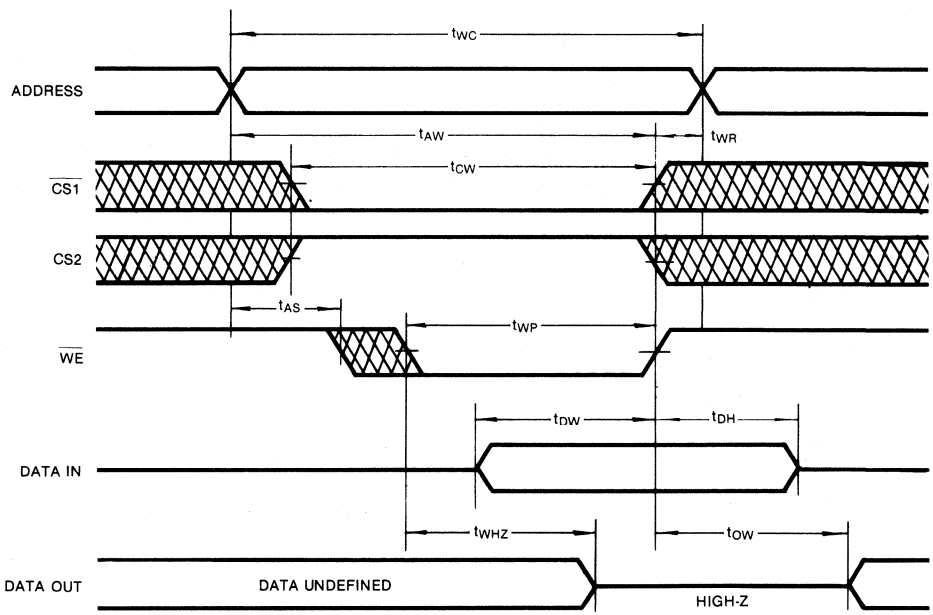
TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{WE}$ = V_{IH})



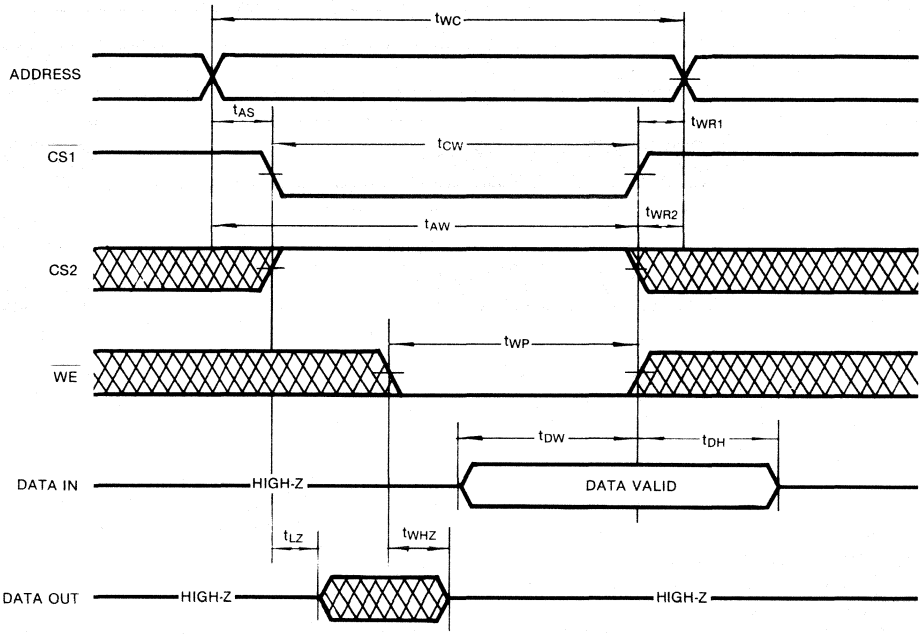
Note (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.

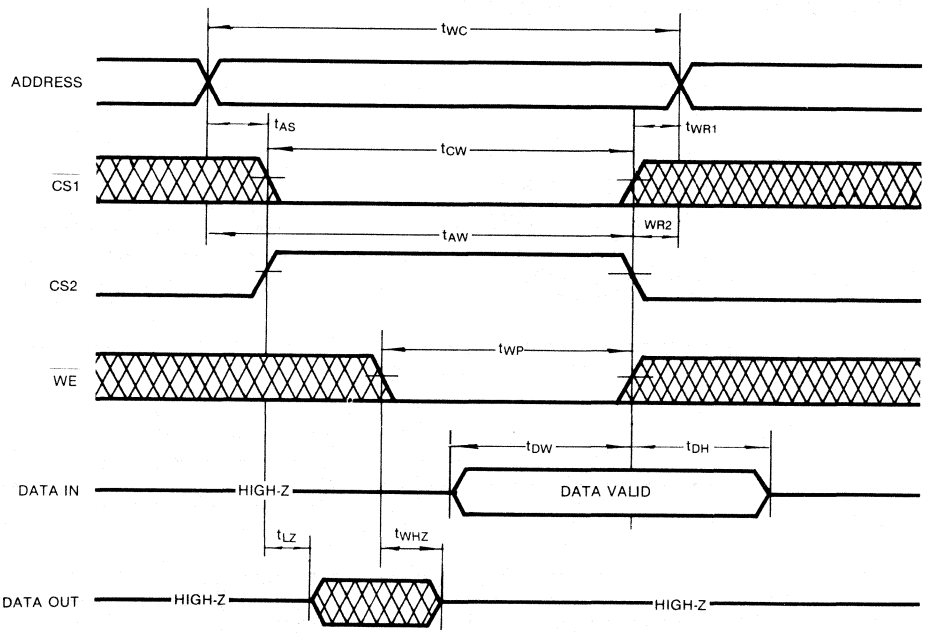
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X*	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

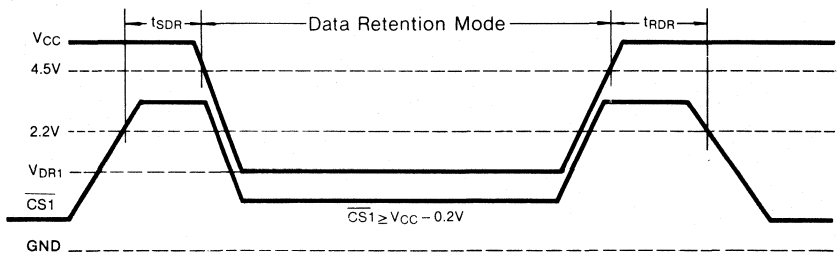
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

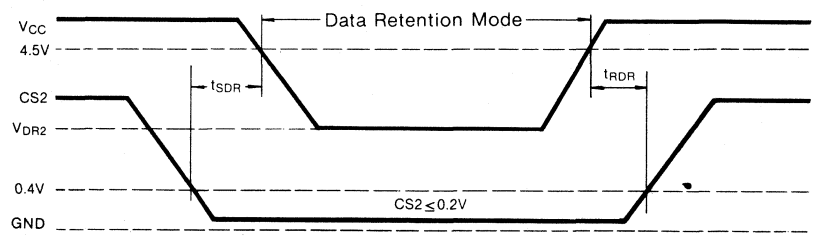
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC} - 0.2V$*		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3V $\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	L		1	50	μA
			LL		0.5	5**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}***			ns

* $\overline{CS1} \geq V_{CC}$-0.2V, $CS2 \geq V_{CC}$-0.2V ($\overline{CS1}$ Controlled) or $CS2 \leq 0.2V$ (CS2 Controlled)
** 1μA (max.) at 0°C~40°C
*** t_{RC}=Read cycle time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



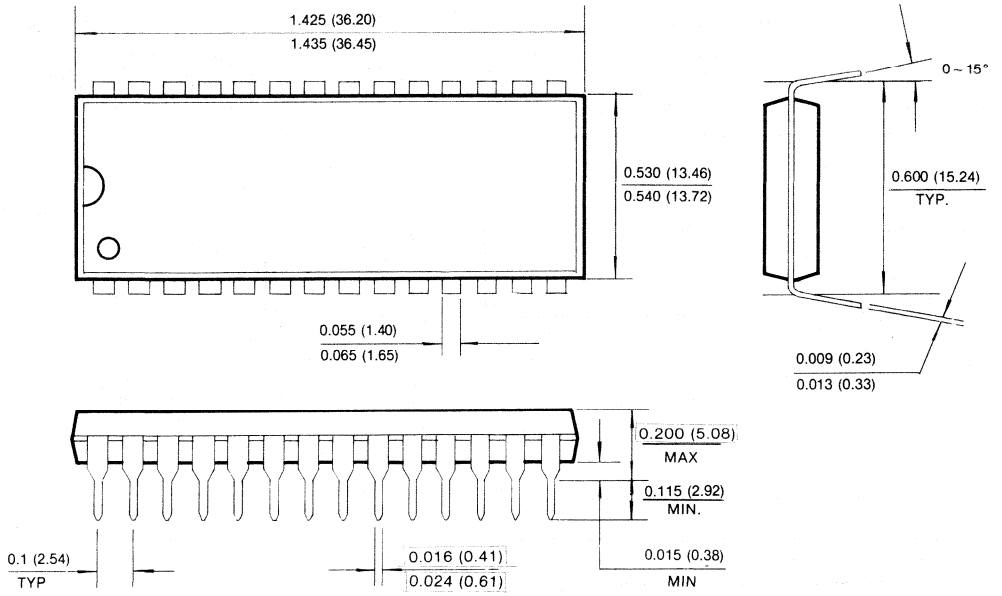
DATA RETENTION WAVEFORM (2) (CS2 Controlled)



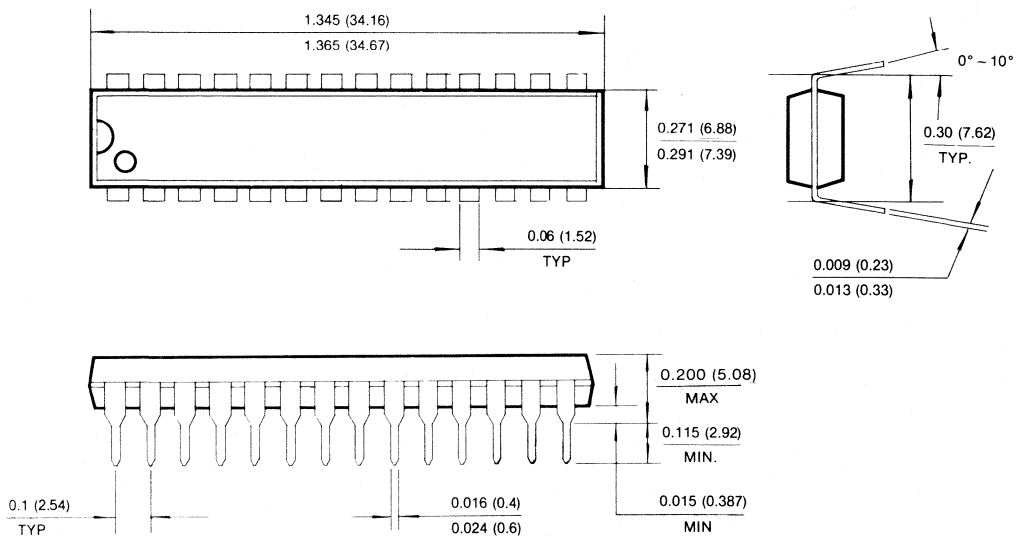
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (Millimeters)



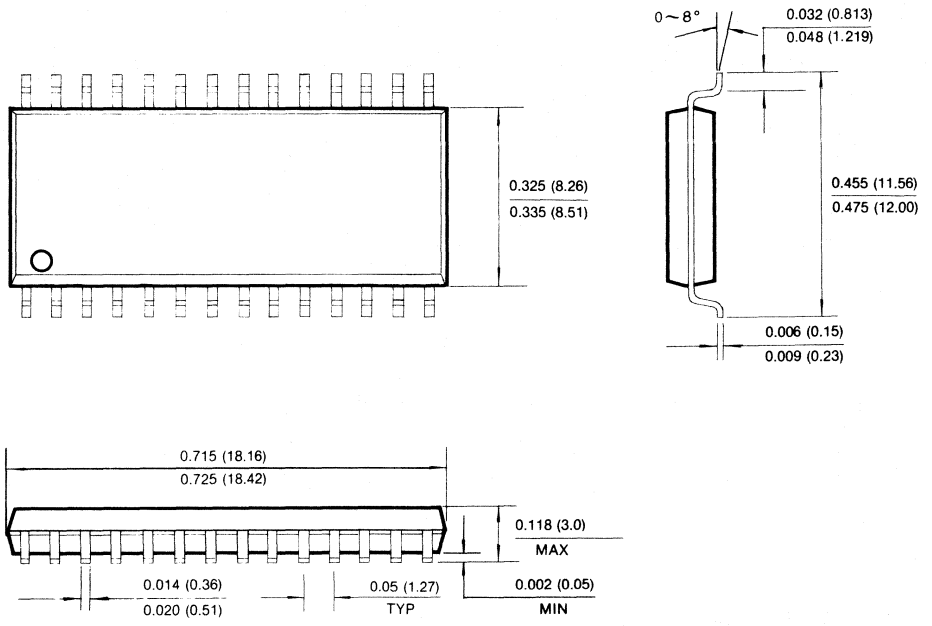
28 PIN PLASTIC DUAL IN LINE PACKAGE (300 mil)



PACKAGE DIMENSIONS (Continued)

28 PIN PLASTIC SMALL OUT LINE PACKAGE (330 mil)

Unit: Inches (Millimeters)



32K x 8 Bit Static RAM

FEATURES

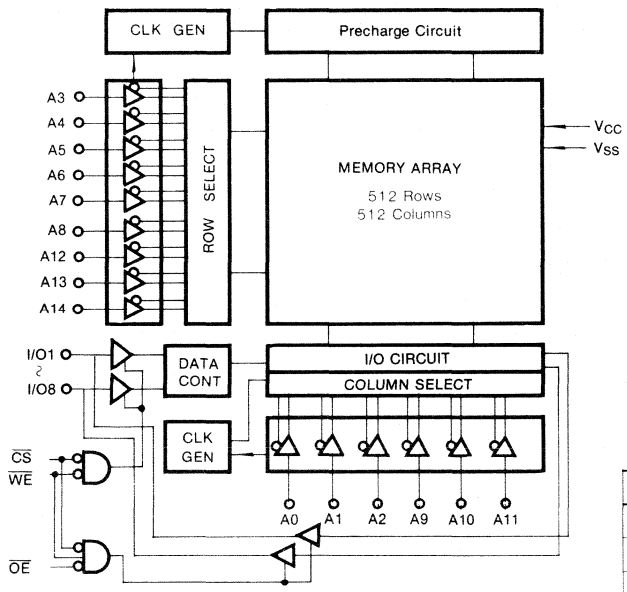
- **Fast Access Time: 80,100,120 ns (max.)**
- **Low Power Dissipation**
  Standby (CMOS): 10μW (typ.) L/LL-Version
  Operating: 247.5mW (max.)
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  —No clock or refresh required
- **Three State Output**
- **Low Data Retention Voltage: 2V (min.)**
- **JEDEC Standard pin Configuration**
  KM62256AP/ALP/ALP-L: 28-pin DIP (600 mil.)
  KM62256AG/ALG/ALG-L: 28-pin SOP (330 mil.)

GENERAL DESCRIPTION

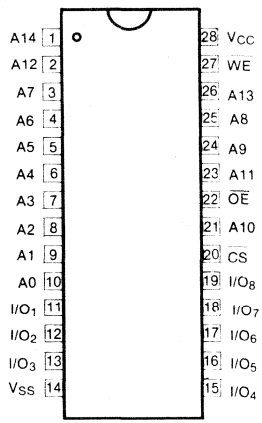
The KM62256A/AL/AL-L is 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bit.
The device is fabricated using Samsung's advanced CMOS technology with polyresistors.
The KM62256A/AL/AL-L has an output enable input for precise control of the data outputs. It also has a chip select input for the minimum current power down mode.
The KM62256A/AL/AL-L has been designed for high speed and low power applications.
It is particularly well suited for battery back-up non-volatile memory applications.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Input/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*		0.8	V

* V_{IL}(min.) = −3.0V for ≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}		−1		1	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL} $I_{I/O}$ = 0mA				45	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty, $\overline{CS}$ = V_{IL} $I_{I/O}$ = 0mA			35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}				2	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V				1	mA
			L		2	100	μA
			LL		2	50	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA				0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1mA		2.4			V

* Typ.: V_{CC} = 5V, Ta = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

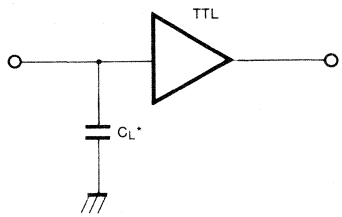
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS ($Ta = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 100pF + 1$ TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256A-8 KM62256AL-8 KM62256AL-8L		KM62256A-10 KM62256AL-10 KM62256AL-10L		KM62256A-12 KM62256AL-12 KM62256AL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80		100		120		ns
Address Access Time	t_{AA}		80		100		120	ns
Chip Select to Output	t_{CO}		80		100		120	ns
Output Enable to Valid Output	t_{OE}		40		50		60	ns
Chip Enable to Low-Z Output	t_{LZ}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	5		10		10		ns

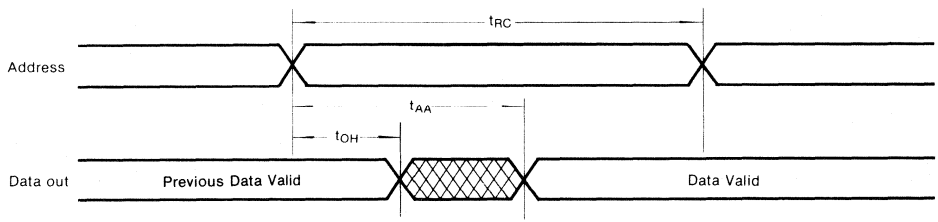
WRITE CYCLE

Parameter	Symbol	KM62256A-8 KM62256AL-8 KM62256AL-8L		KM62256A-10 KM62256AL-10 KM62256AL-10L		KM62256A-12 KM62256AL-12 KM62256AL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80		100		120		ns
Chip Select to End of Write	t_{CW}	70		80		85		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	70		80		85		ns
Write Pulse Width	t_{WP}	55		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	40		50		60		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		10		10		ns

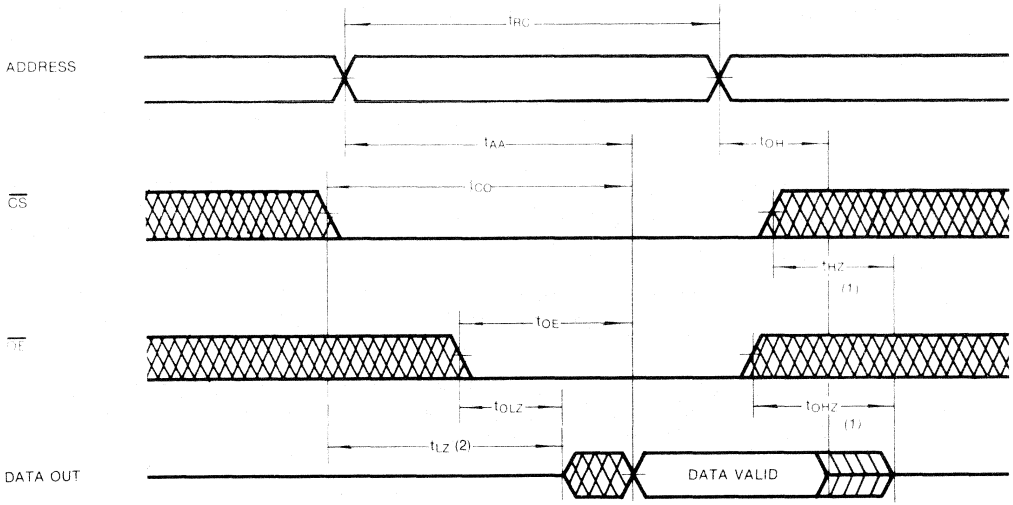
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO: 1

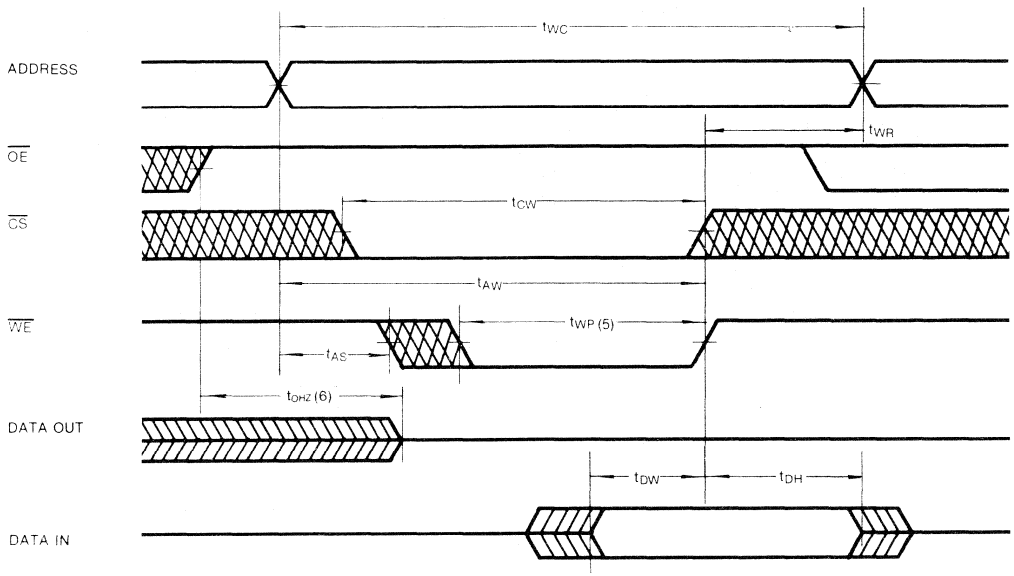
($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



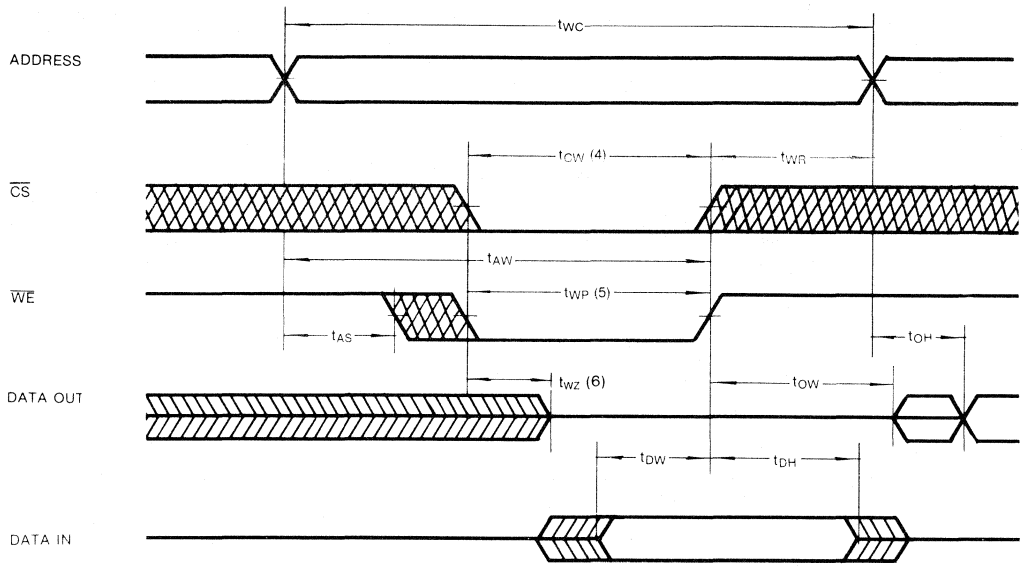
TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 4 ($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} Level.
2. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for Read Cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

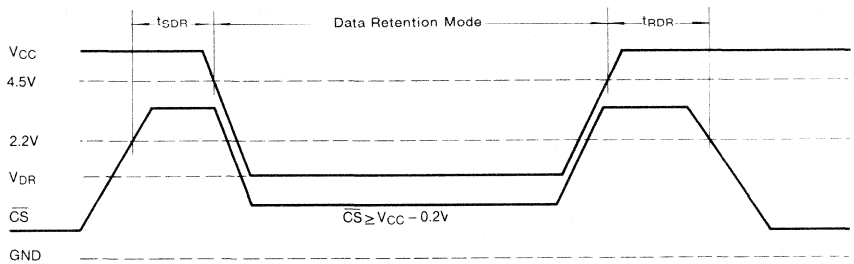
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3V $\overline{CS} \geq V_{CC} - 0.2V$	L		1	50	μA
			LL		1	20 *	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC} **			ns

* 3μA (max.) at 0°C ~ 40°C
** t_{RC} = Read cycle time

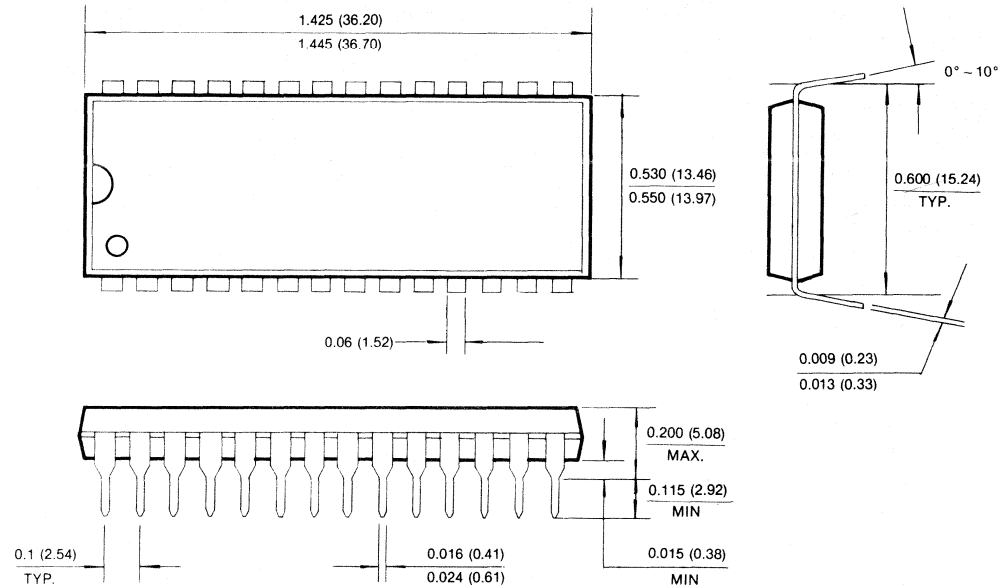
DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



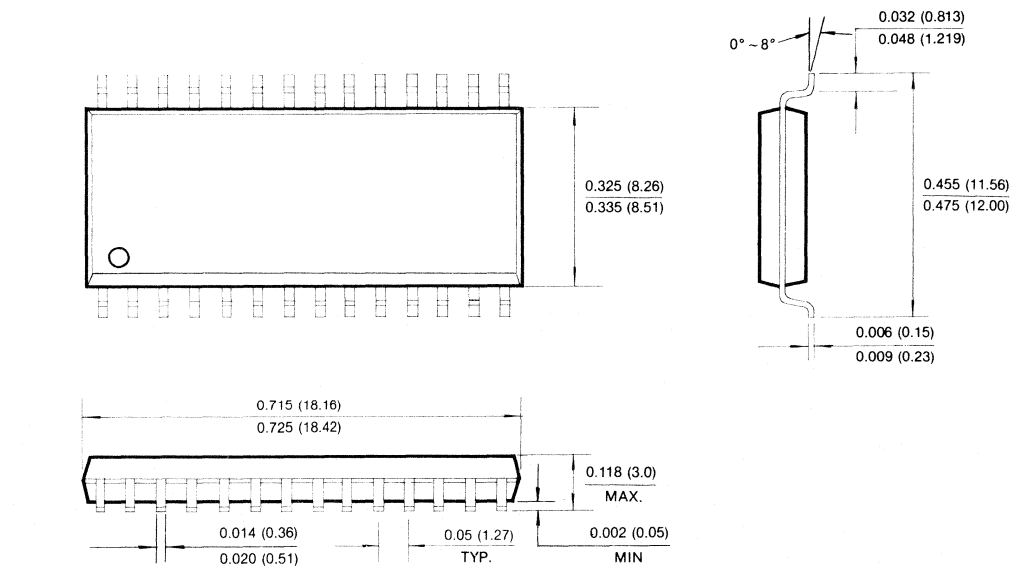
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE PACKAGE



32,768 WORD x 8 Bit CMOS Static RAM

FEATURES

- **Fast Access Time: 70, 85, 100, 120ns (Max.)**
- **Low Power Dissipation**
  - **Standby (CMOS): 10μW (Typ.) L-Version**
  - **5μW (Typ.) LL-Version**
  - **Operating : 35mW (Typ.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (Min.)**
- **Standard Pin Configuration**
  - **KM62256BLP/BLP-L: 28-pin DIP**
  - **KM62256BLG/BLG-L: 28-pin SOP**
  - **KM62256BLS/BLS-L: 28-Pin SDIP**
  - **KM62256BLT/BLT-L: 32-pin TSOP, Standard**
  - **KM62256BLR/BLR-L: 32-pin TSOP, Reverse**
  - **KM62256BLTG/BLTG-L: 28-pin TSOP, Standard**
  - **KM62256BLRG/BLRG-L: 28-pin TSOP, Reverse**

GENERAL DESCRIPTION

The KM62256BL/BL-L is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS process with polyresistors.

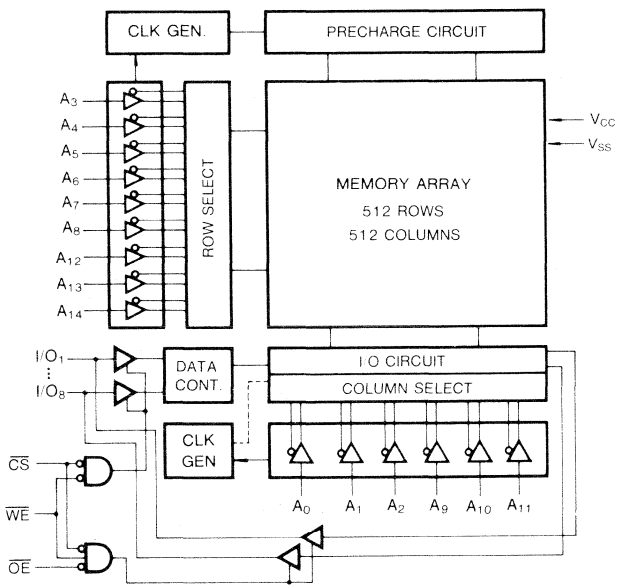
The KM62256BL/BL-L has an output enable input for precise control of the data outputs.

It also has a chip enable input for the minimum current power down mode.

The KM62256BL/BL-L has been designed for high speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

2

FUNCTIONAL BLOCK DIAGRAM

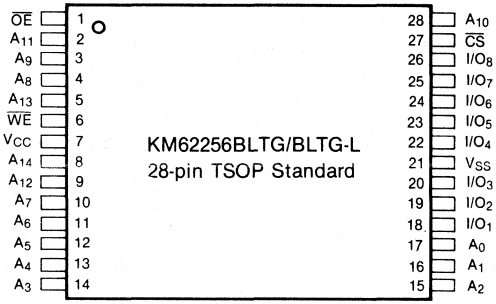


PIN CONFIGURATIONS

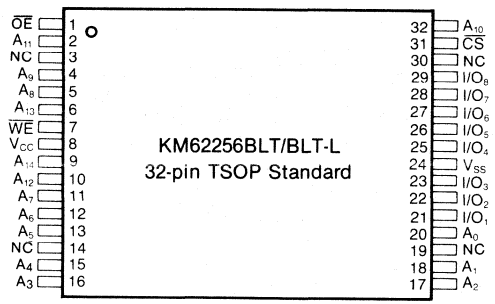
Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection (32-TSOP only)

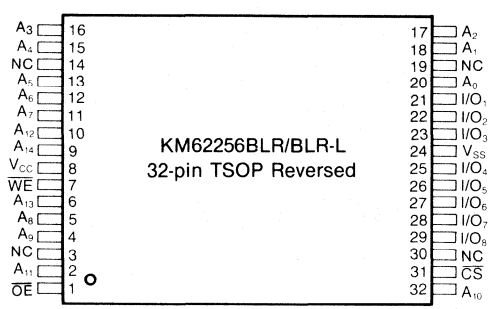
PIN CONFIGURATIONS (Top View)

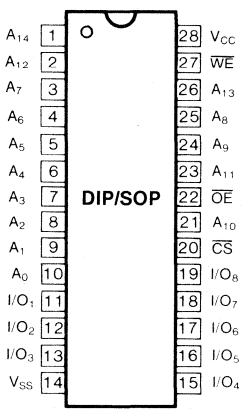
28-pin TSOP (0813.4)



32-pin TSOP (0814)







ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to V_{CC} + 0.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min) = −3.0V for ≤50ns Pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}		−1	—	1	μA
Operation Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL}, $I_{I/O}$ = 0mA		—	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, 100% Duty, $\overline{CS} \le 0.2V$, $V_{IL} \le 0.2V$, $V_{IH} \ge V_{CC} - 0.2V$, $I_{I/O}$ = 0mA		—	—	7	mA
	I_{CC2}	Min Cycle, 100% Duty, $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA		—	45	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$		—	—	1	mA
	I_{SB1}	$\overline{CS} \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$	L-Ver.	—	2	100	μA
			LL-Ver.	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

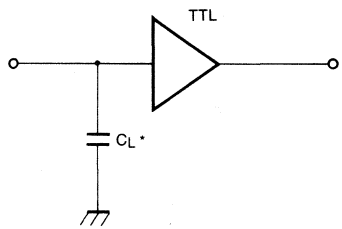
CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Loads	$C_L = 100pF + 1$ TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256BL-7 KM62256BL-7L		KM62256BL-8 KM62256BL-8L		KM62256BL-10 KM62256BL-10L		KM62256BL-12 KM62256BL-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Chip Select to Output	t_{CO}		70		85		100		120	ns
Output Enable to Valid Output	t_{OE}		35		45		50		60	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5		ns
Chip Disselect to High-Z Output	t_{HZ}	0	30	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	5		5		10		10		ns

WRITE CYCLE

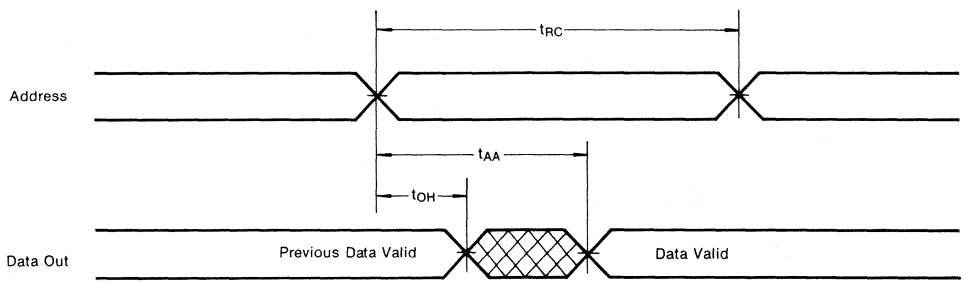
Parameter	Symbol	KM62256BL-7 KM62256BL-7L		KM62256BL-8 KM62256BL-8L		KM62256BL-10 KM62256BL-10L		KM62256BL-12 KM62256BL-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		85		ns
Address Valid to End of Write	t_{AW}	0		0		0		0		ns
Address Set-up Time	t_{AS}	60		75		80		85		ns
Write Pulse Width	t_{WP}	50		60		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	0	30	0	40	ns
Data to Write Time Overlap	t_{DW}	30		40		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		5		ns

2

TIMING DIAGRAMS

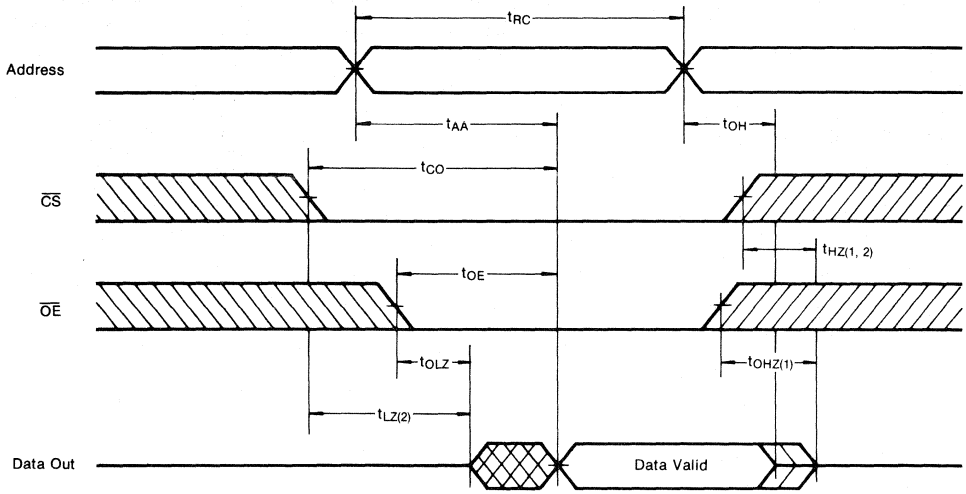
TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



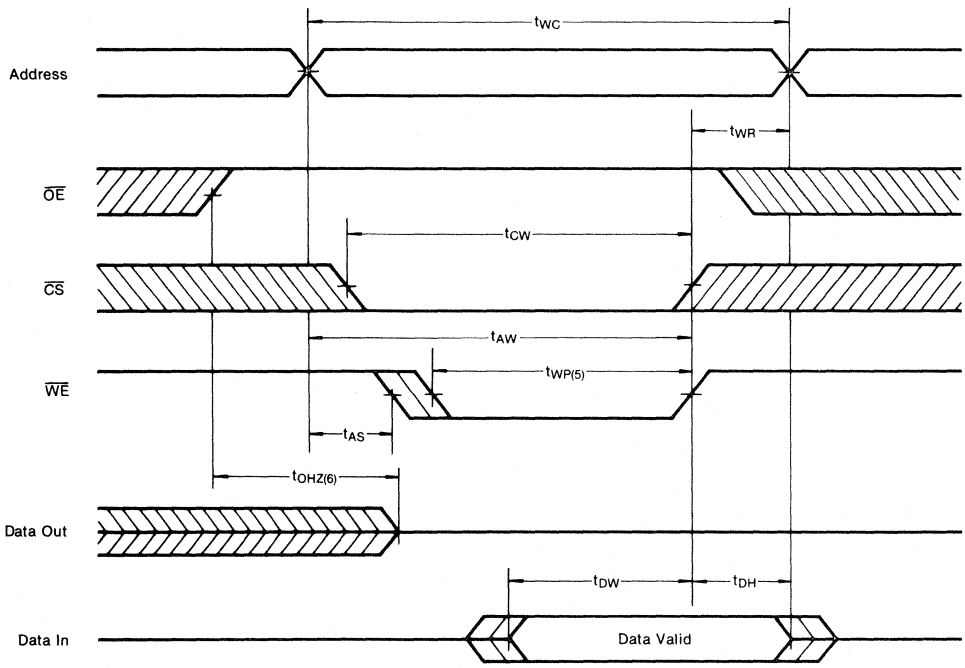
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



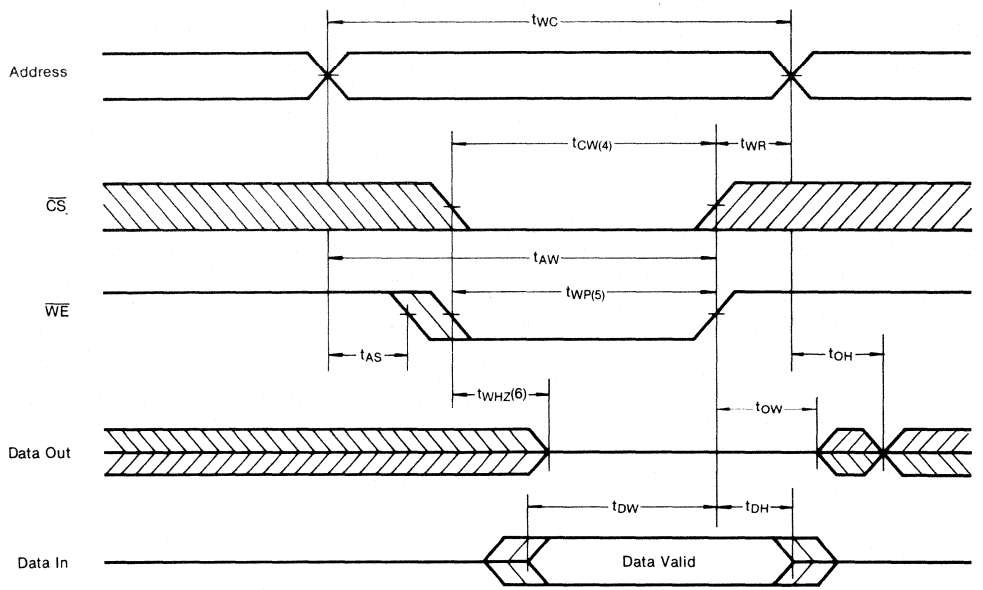
TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

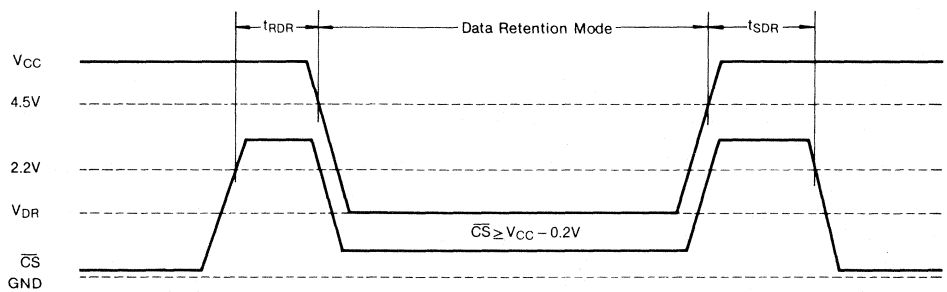
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V $\overline{CS} \geq V_{CC} - 0.2V$	L		1	50*	μA
			L-L		0.5	10**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}***			ns

* 20μA (Max.) at 0°C ~ 40°C
** 3μA (Max.) at 0°C ~ 40°C
*** t_{RC}: Read Cycle Time

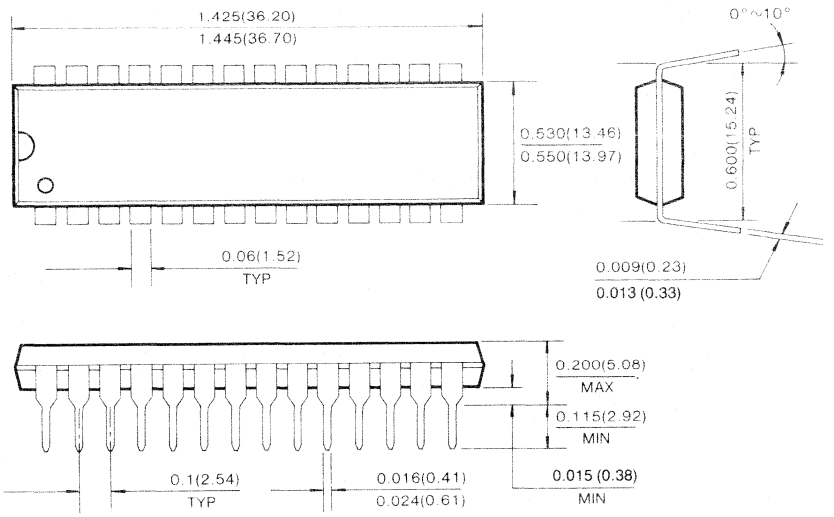
DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



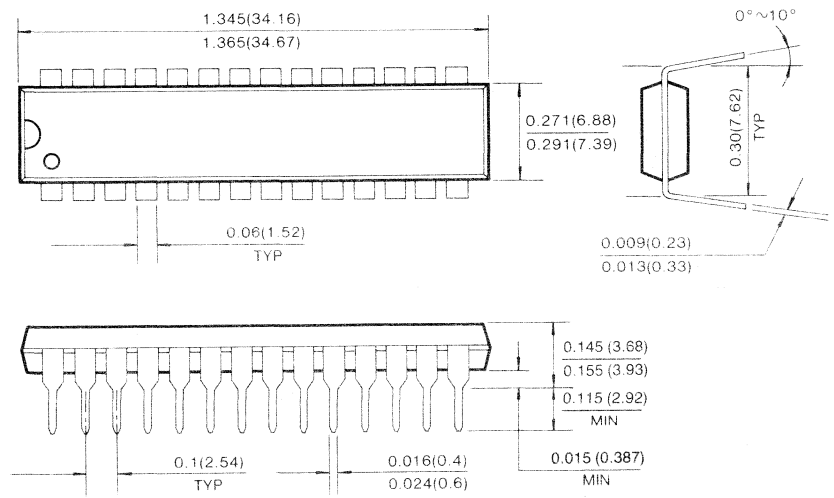
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (Millimeters)



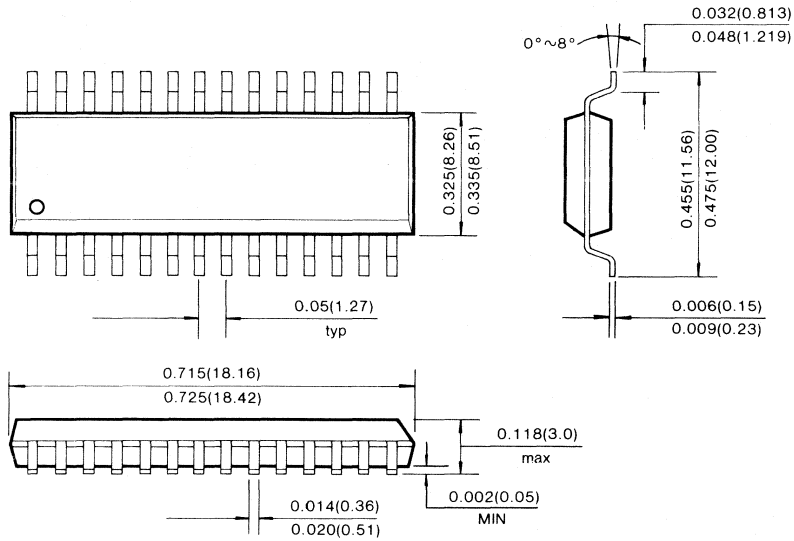
28 PIN PLASTIC DUAL IN LINE PACKAGE (300 mil)



PACKAGE DIMENSIONS (Continued)

28 PIN PLASTIC SMALL OUT LINE PACKAGE (330 mil)

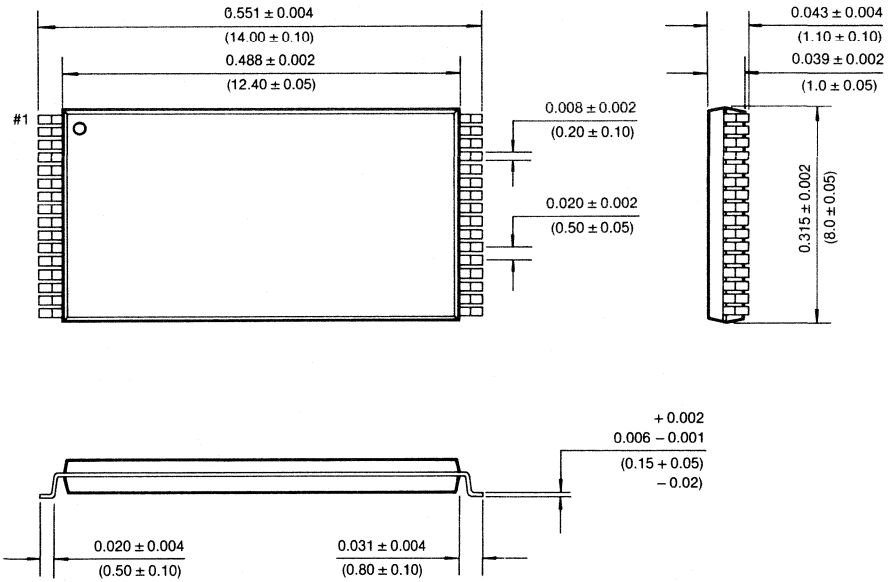
Units: Inches (millimeters)



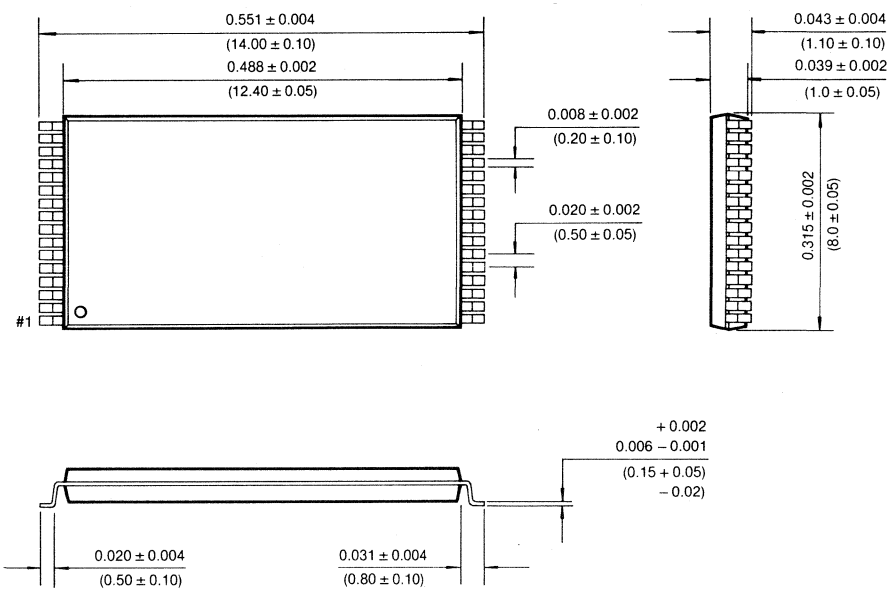
PACKAGE DIMENSIONS

32 PIN THIN SMALL OUTINE PACKAGE (0814F)

Unit: Inches (millimeters)

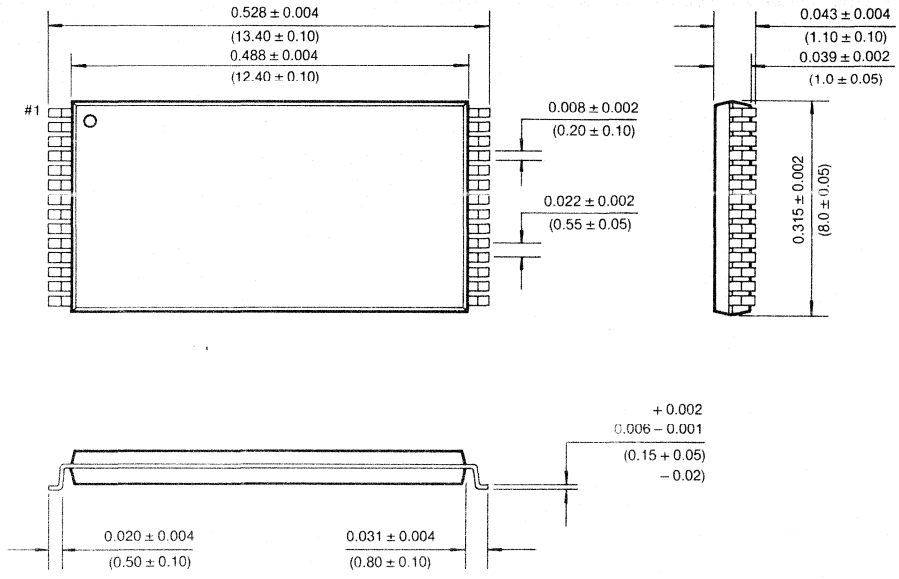


32 PIN THIN SMALL OUTLINE PACKAGE (0814R)

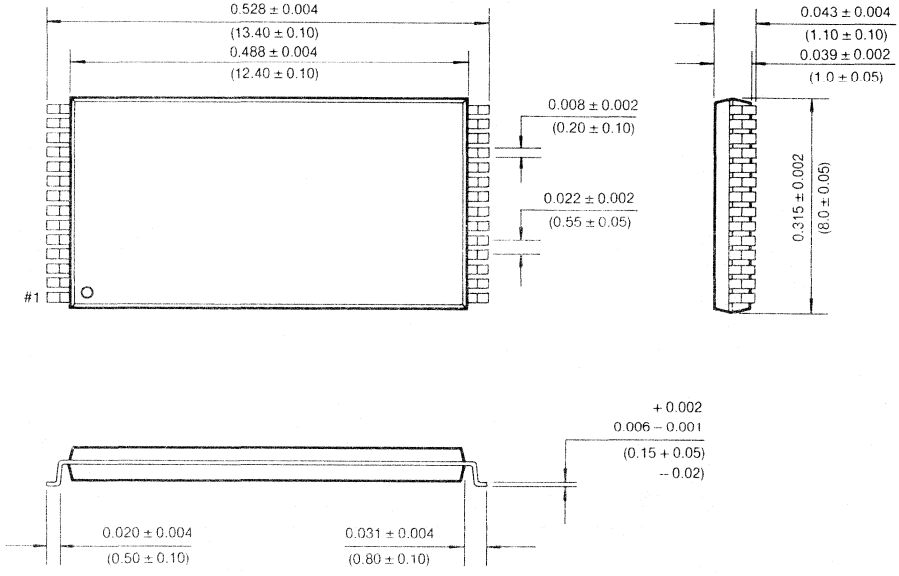


28 PIN THIN SMALL OUTLINE PACKAGE (0813.4F)

Unit: Inches (millimeters)



28 PIN THIN SMALL OUTLINE PACKAGE (0813.4R)



32,768 WORD×8 Bit CMOS Static RAM

FEATURES

- Industrial Temperature Range: −40 to 85°C
- Fast Access Time: 70, 100ns (Max.)
- Low Power Dissipation
  - Standby (CMOS): 275μW (Max.)
  - Operating : 110mW (Max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No clock or refresh required
- Three State Outputs
- Low Data Retention Voltage: 2V (Min.)
- JEDEC Standard Pin Configuration
  - KM62256BLPI: 28-pin DIP (600mil)
  - KM62256BLGI: 28-pin SOP (330mil)

GENERAL DESCRIPTION

The KM62256BLPI/BLGI is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS technology. The KM62256BLPI/BLGI has an output enable input for precise control of the data outputs.

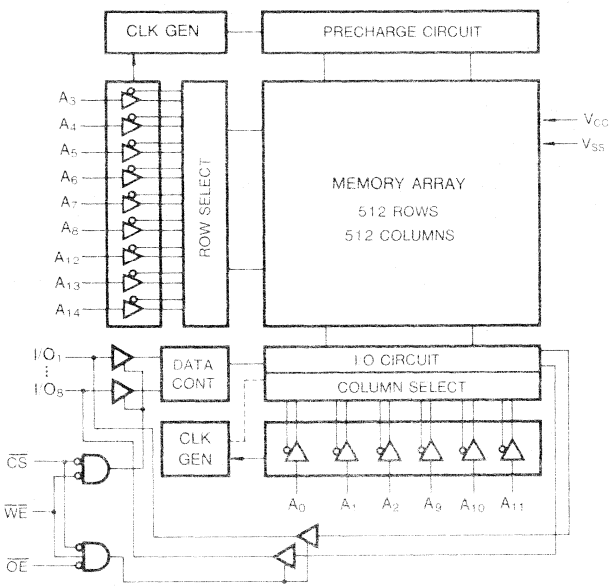
It also has a chip enable input for the minimum current power down mode.

The KM62256BLPI/BLGI has been designed for high speed and low power application. It is particularly well suited for battery back-up memory application.

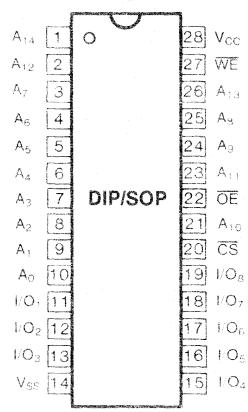
And −40 to 85°C operating temperature range makes it ideal for industrial use.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	−40 to 85	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = −40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min) = −3.0V for ≤50ns Pulse

DC AND OPERATING CHARACTERISTICS

(T_A = −40 to 85°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}		−1	—	1	μA
Operation Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		—	7	20	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, 100% Duty, $\overline{CS}$ ≤ 0.2V, V_{IL} ≤ 0.2V, V_{IH} ≥ V_{CC} − 0.2V, $I_{I/O}$ = 0mA		—	—	10	mA
	I_{CC2}	Min. Cycle, 100% Duty, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA		—	—	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}		—	—	2	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	T_A = −40 ~ 85°C	—	1	50	μA
			T_A = 25°C	—	—	2	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

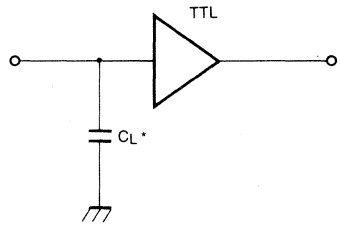
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 100pF + 1$ TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256BLPI-7 KM62256BLGI-7		KM62256BLPI-10 KM62256BLGI-10		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO}		70		100	ns
Output Enable to Valid Output	t_{OE}		35		50	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Disselect to High-Z Output	t_{HZ}	0	30	0	35	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	ns
Output Hold from Address Change	t_{OH}	5		10		ns

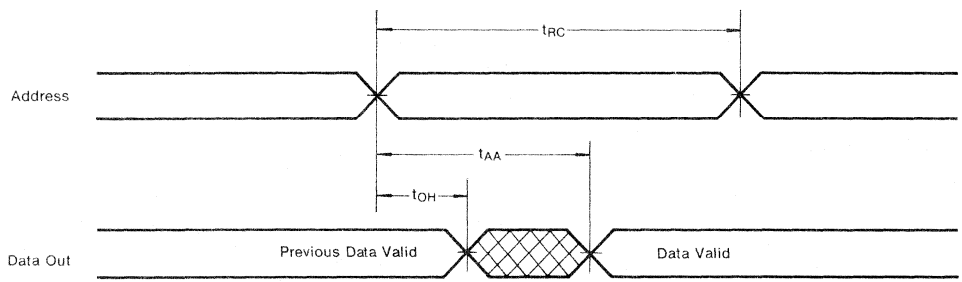
WRITE CYCLE

Parameter	Symbol	KM62256BLPI-7 KM62256BLGI-7		KM62256BLPI-10 KM62256BLGI-10		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		ns
Chip Select to End of Write	t_{CW}	60		80		ns
Address Valid to End of Write	t_{AW}	60		80		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	50		60		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	35	ns
Data to Write Time Overlap	t_{DW}	30		50		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	5		10		ns

TIMING DIAGRAMS

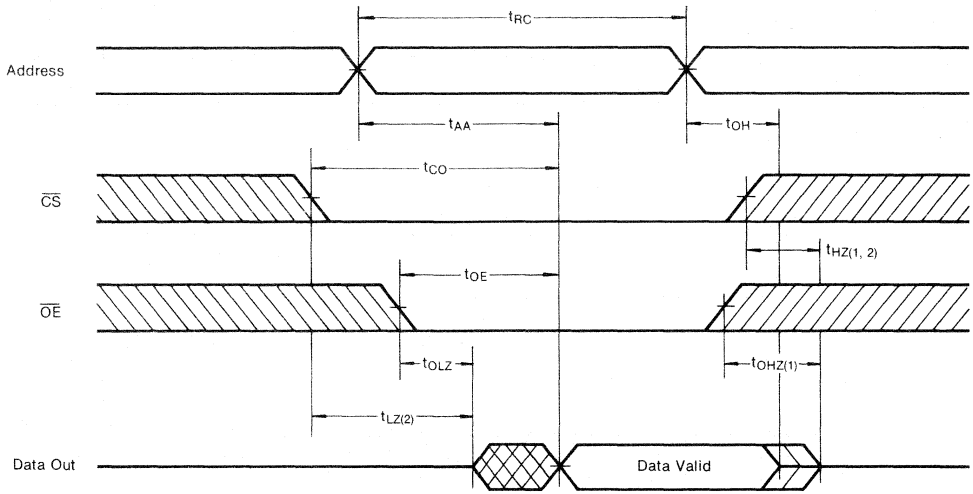
TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



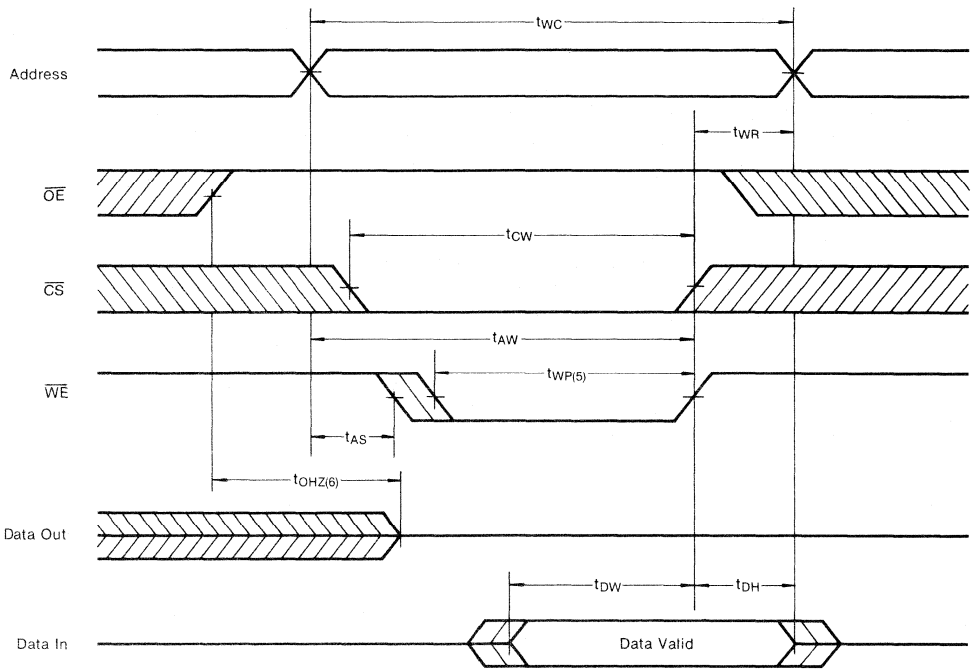
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



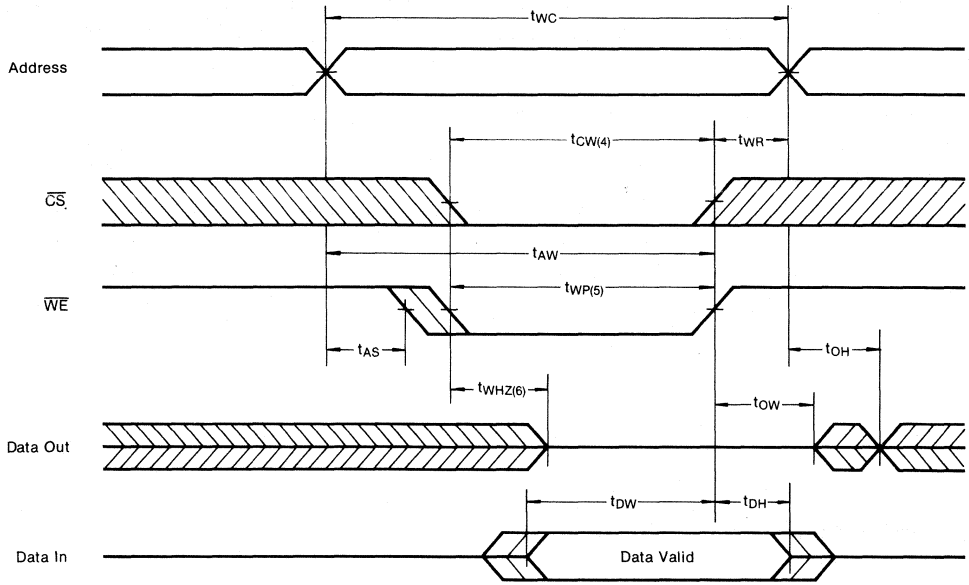
TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

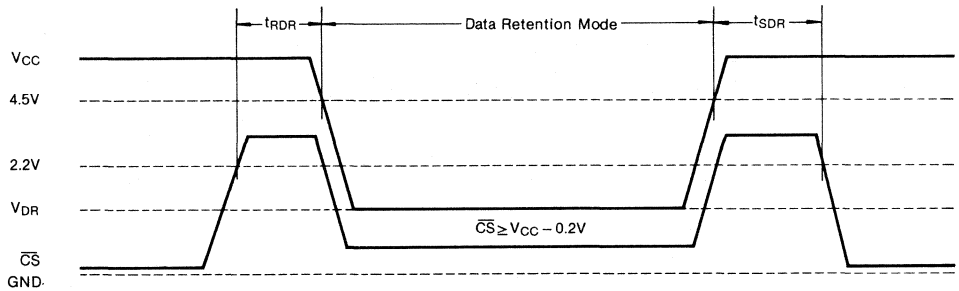
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = −40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		0.5	20	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

* t_{RC}: Read Cycle Time

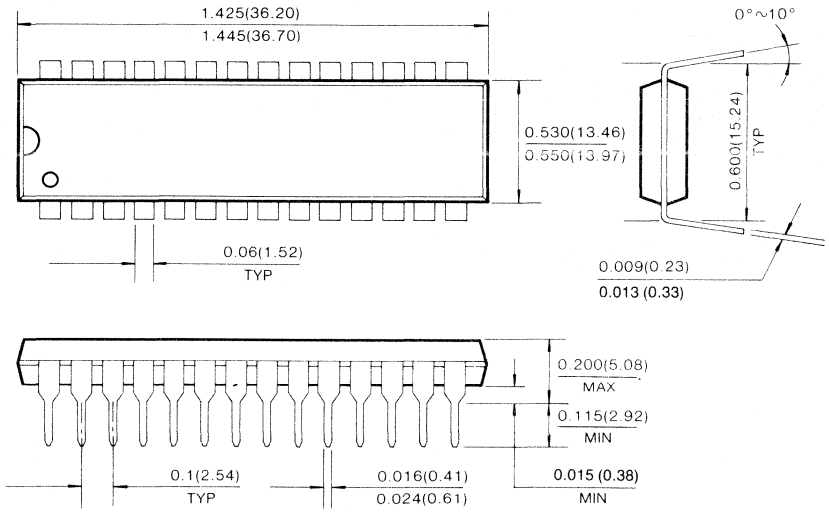
DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



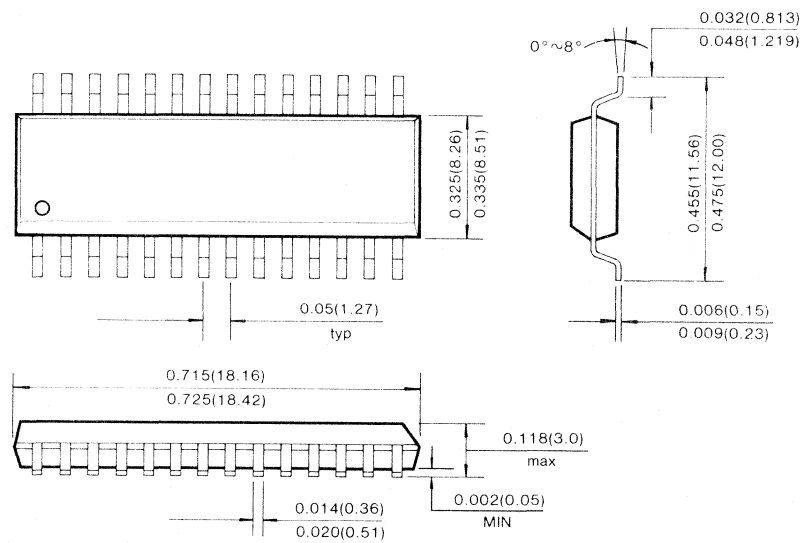
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (millimeters)



28 PIN PLASTIC SMALL OUTLINE PACKAGE (330 mil)



32,768 WORD×8 Bit CMOS Static RAM

FEATURES

- Extended Operating Voltage: 2.7~5.5V
- Fast Access Time:
  - 3V Operation: 240ns (Max.)
  - 5V Operation: 120ns (Max.)
- Low Power Dissipation Standby/Operating
  - 3V Operation: 2.4μW/1.2mW (Typ.)
  - 5V Operation: 5.0μW/35mW (Typ.)
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No clock or refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM62256BLP-V: 28-pin DIP (600mil)
  - KM62256BLS-V: 28-pin SDIP (300mil)
  - KM62256BLG-V: 28-pin SOP (330mil)
  - KM62256BLT-V: 32-pin TSOP with Reverse
  - KM62256BLTG-V: 28-pin TSOP with Reverse

GENERAL DESCRIPTION

The KM62256BL-V is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS process and high-speed circuit technology.

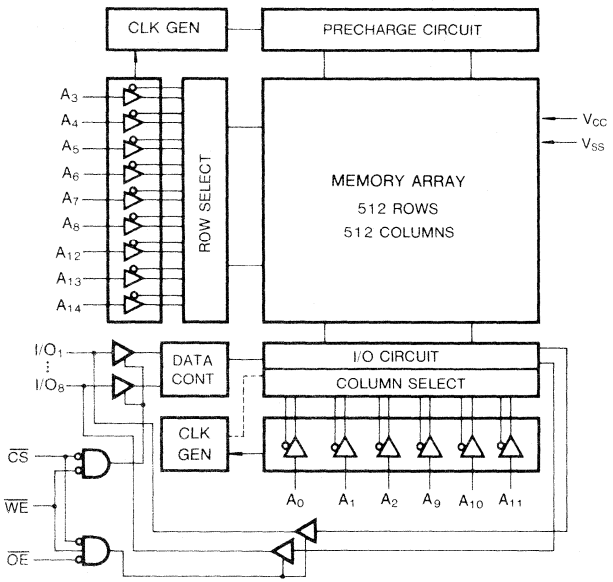
The KM62256BL-V has an output enable input for precise control of the data outputs.

It also has a chip enable input for the minimum current power down mode.

The KM62256BL-V is particulary well suited for use in low voltage (2.7~5.5V) operation and battery back-up applications.

2

FUNCTIONAL BLOCK DIAGRAM

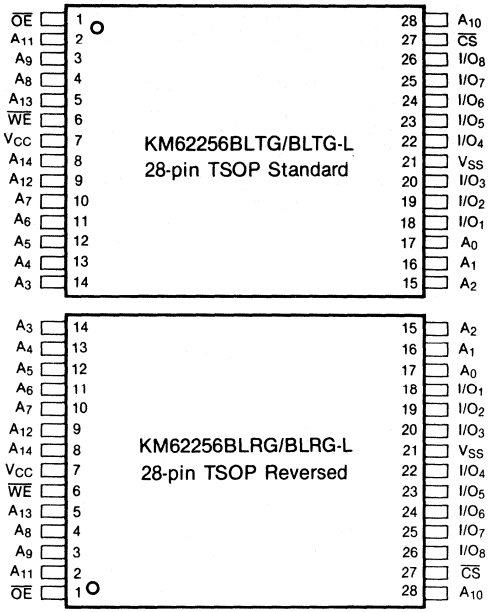


PIN CONFIGURATIONS

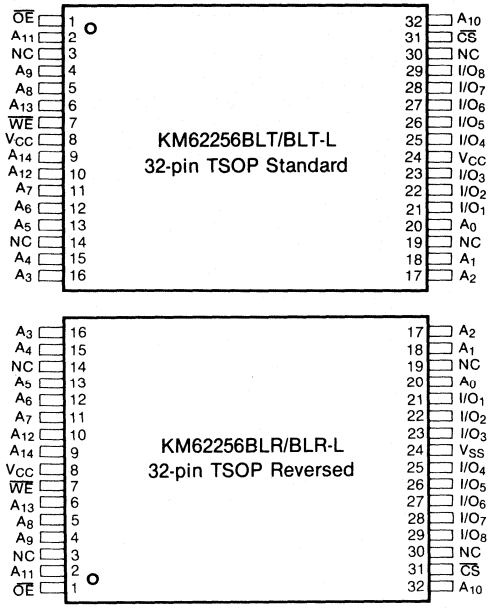
Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (2.7~5.5V)
V_{SS}	Ground
N.C.	No Connection (32-TSOP only)

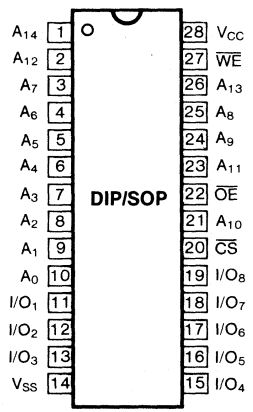
PIN CONFIGURATIONS (Top View)

28-pin TSOP (0813.4)



32-pin TSOP (0814)





ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to $V_{CC}+0.5$	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS ($T_A=0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	-0.5*	—	0.4	V

* V_{IL}(min.) = -3.0V for $\leq$50ns pulse

DC AND OPERATING CHARACTERISTICS

($T_A=0$ to 70°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	$V_{CC}=3V\pm10\%$			$V_{CC}=5V\pm10\%$			Unit
			Min	Typ*	Max	Min	Typ**	Max	
Input Leakage Current	I_{LI}	$V_{IN}=V_{SS}$ to V_{CC}	-0.5	—	0.5	-1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IL}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	-0.5	—	0.5	-1	—	1	μA
Operation Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $V_{IN}=V_{IH}$ or V_{IL} $I_{I/O}=0$mA	—	0.4	0.8	—	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, 100% Duty $\overline{CS}\leq0.2$V, $V_{IL}\leq0.2$V, $V_{IH}\geq V_{CC}-0.2$V, $I_{I/O}=0$mA	—	2.5	5	—	—	7	mA
	I_{CC2}	Min Cycle, 100% Duty $\overline{CS}=V_{IL}$, $I_{I/O}=0$mA	—	10	15	—	45	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	—	0.3	—	—	1	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2$V, $V_{IN}\geq V_{CC}-0.2$V or $V_{IN}\leq0.2$V	—	0.8	20	—	1	50	μA
Output Low Voltage	V_{OL}	$I_{OL}=2.1$mA	—	—	0.4	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-1.0$mA	2.2	—	—	2.4	—	—	V

* Typ: $V_{CC}=3V$, $T_A=25$°C
** Typ: $V_{CC}=5V$, $T_A=25$°C

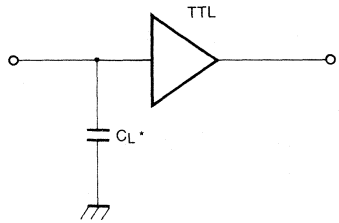
CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 3V \pm 10\%$, unless otherwise specified)

Parameter	Value	
	$V_{CC} = 3.0V$	$V_{CC} = 5.0V$
Input Pulse Level	2.2V/0.4V	2.4V/0.8V
Input Rise and Fall Time	5ns	5ns
Input and Output Timing Reference Levels	1.5V	1.5V
Output Load	$C_L = 100pF + 1$ TTL	$C_L = 100pF + 1$ TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	$V_{CC} = 3.0V \pm 10\%$		$V_{CC} = 5.0V \pm 10\%$		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	240		120		ns
Address Access Time	t_{AA}		240		120	ns
Chip Select to Output	t_{CO}		240		120	ns
Output Enable to Valid Output	t_{OE}		120		60	ns
Chip Select to Low-Z Output	t_{LZ}	20		10		ns
Output Enable to Low-Z Output	t_{OLZ}	10		5		ns
Chip Disselect to High-Z Output	t_{HZ}	0	80	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	80	0	40	ns
Output Hold from Address Change	t_{OH}	30		10		ns

WRITE CYCLE

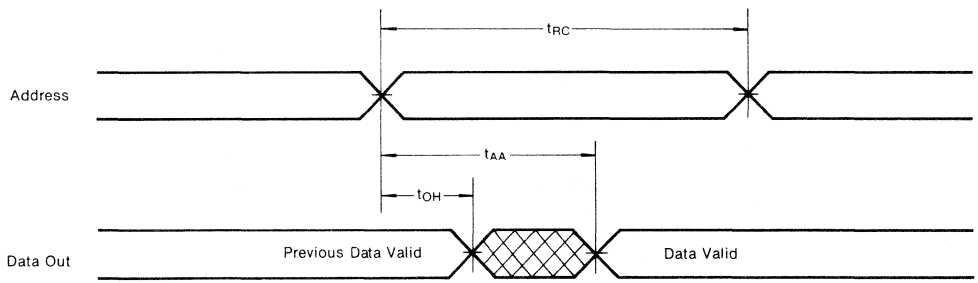
Parameter	Symbol	V_{CC} = 3.0V ± 10%		V_{CC} = 5.0V ± 10%		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	240		120		ns
Chip Select to End of Write	t_{CW}	170		85		ns
Address Valid to End of Write	t_{AW}	170		85		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	160		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	60	0	40	ns
Data to Write Time Overlap	t_{DW}	100		50		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	20		5		ns

2

TIMING DIAGRAMS

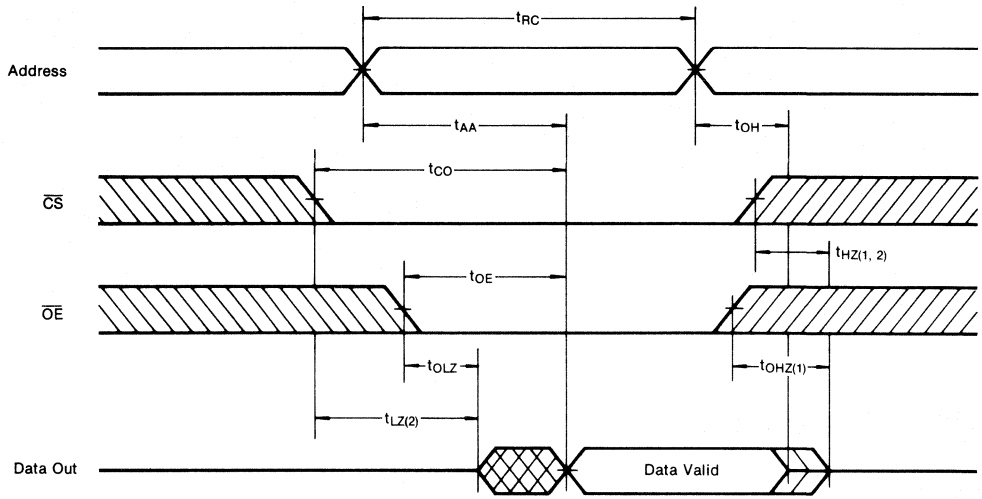
TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



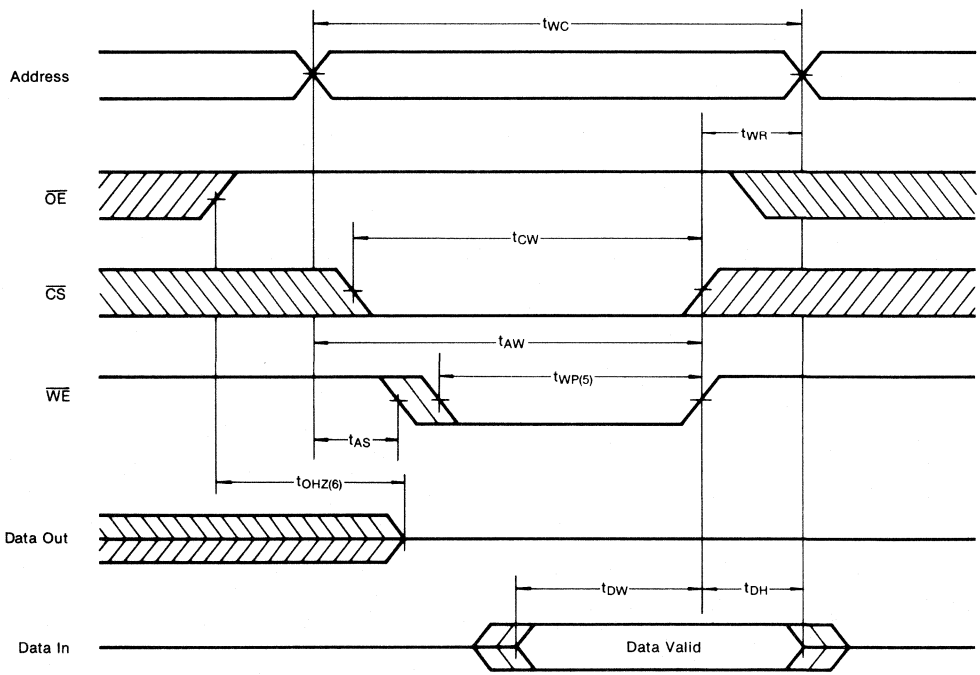
TIMING WAVEFORM OF READ CYCLE (2)

($\overline{WE}$ = V_{IH}) (Note 1, 2, 3, 4)



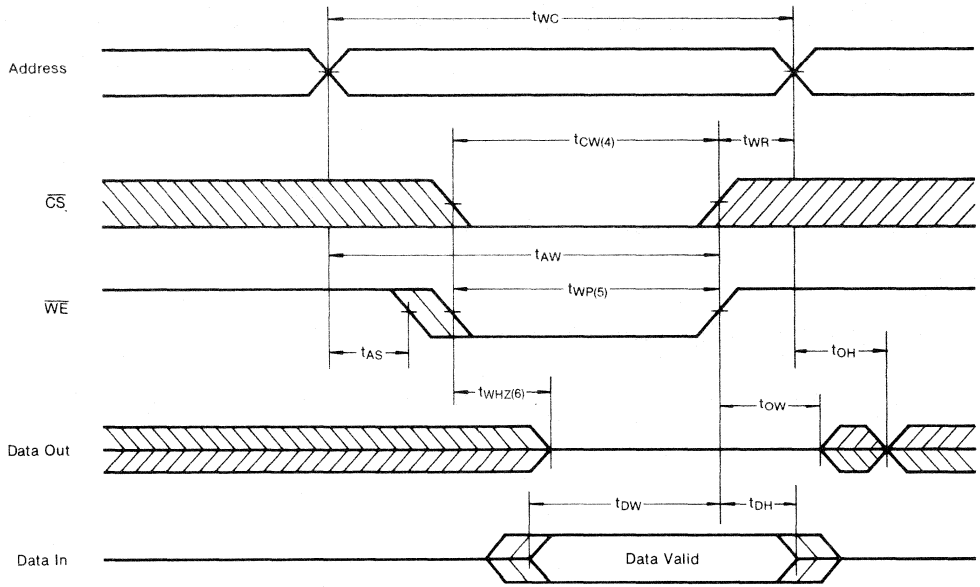
TIMING WAVEFORM OF WRITE CYCLE (3)

($\overline{OE}$ Clocked) (Note 5, 6, 7, 8)



TIMING WAVEFORM OF WRITE CYCLE (4)

($\overline{OE}$ Low Fixed) (Note 5, 6, 7, 8, 9)



Notes

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the V_{OH} or V_{OL} level.
2. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.
5. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and $\overline{WE}$.
6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
7. $\overline{CS}$ or $\overline{WE}$ must be high during address transition state.
8. If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.
9. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

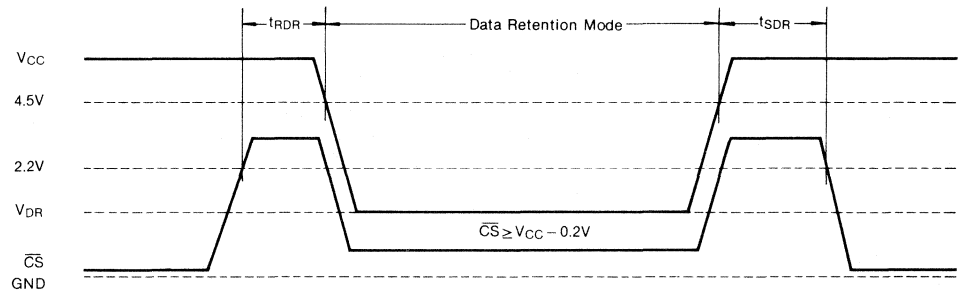
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$		2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$	0~70°C			20	μA
			0~40°C			5	μA
			25°C		0.5	0.8	μA
		$V_{CC} = 2.7 \sim 5.5V$			1*	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}**			ns

*: V_{CC} = 5V, T_A = 25°C
**t_{RC}: Read Cycle Time

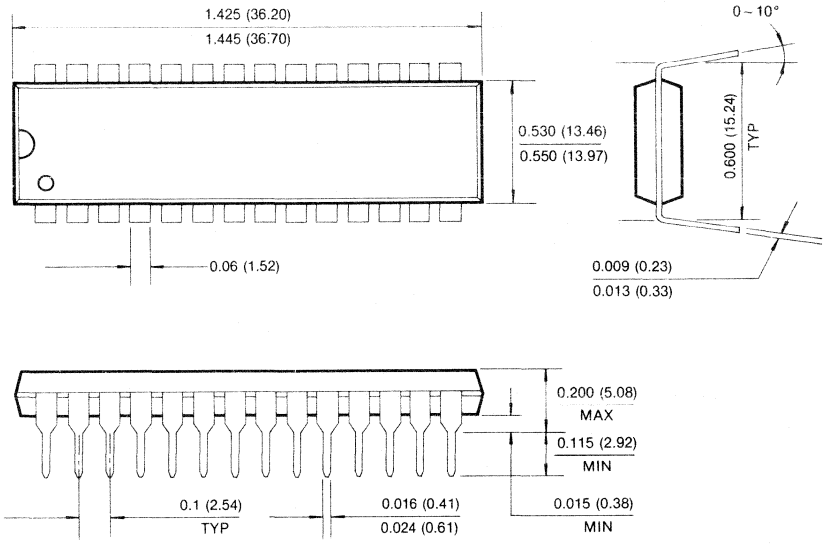
DATA RETENTION WAVEFORM ($\overline{CS}$ Controlled)



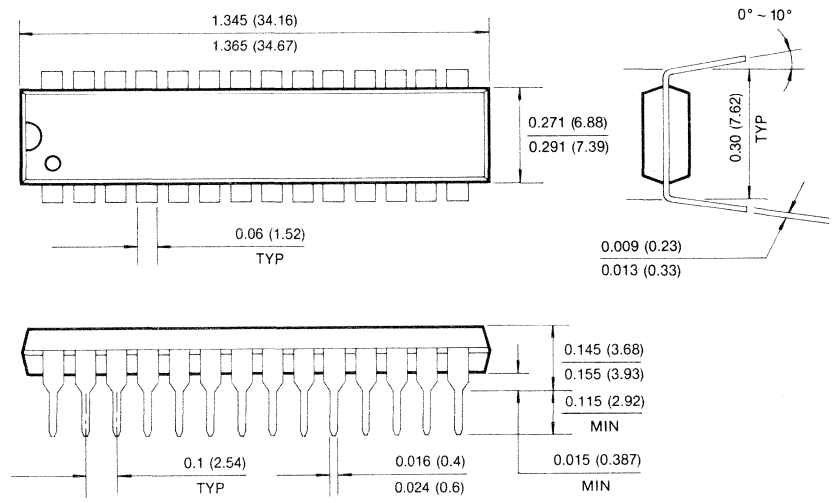
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil.)

Unit: Inches (millimeters)



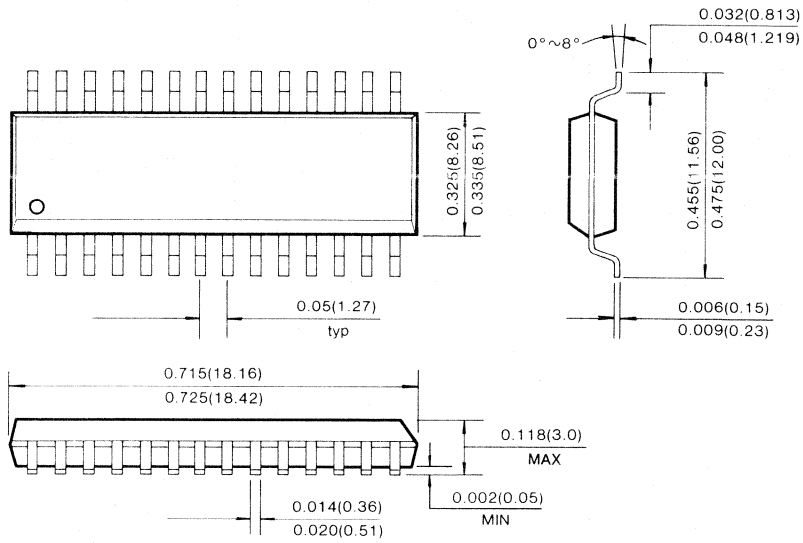
28 PIN PLASTIC DUAL IN LINE PACKAGE (300 mil.)



PACKAGE DIMENSIONS (Continued)

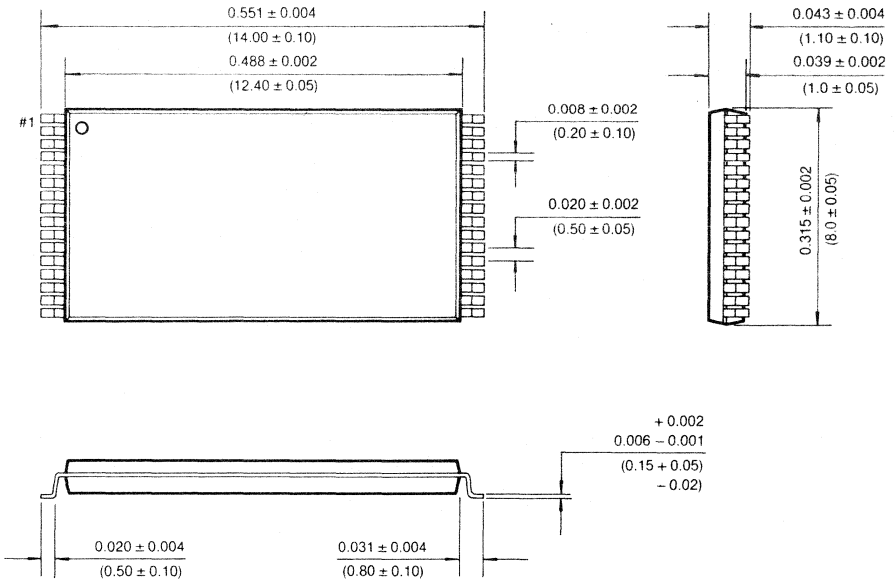
28 PIN PLASTIC SMALL OUT LINE PACKAGE (330 mil.)

Units: Inches (millimeters)

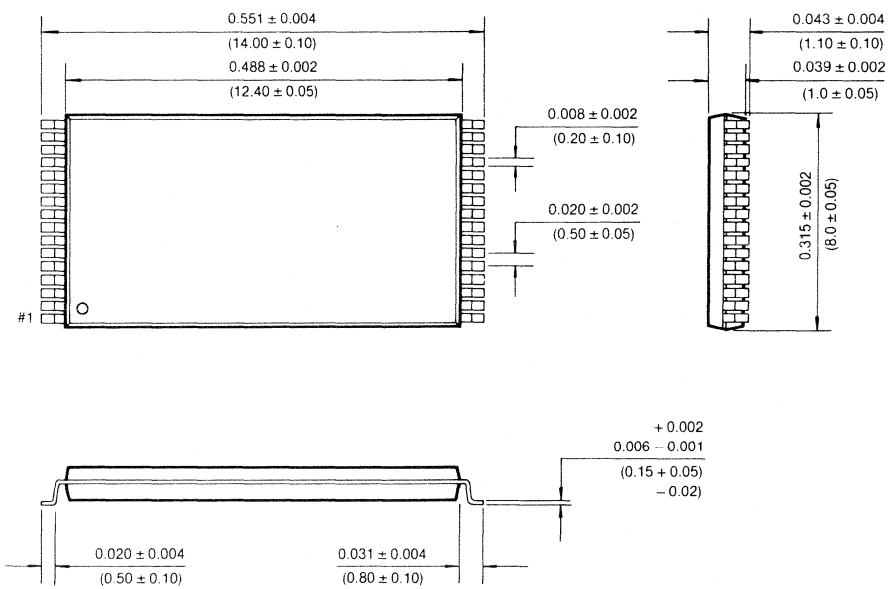


32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0814F)

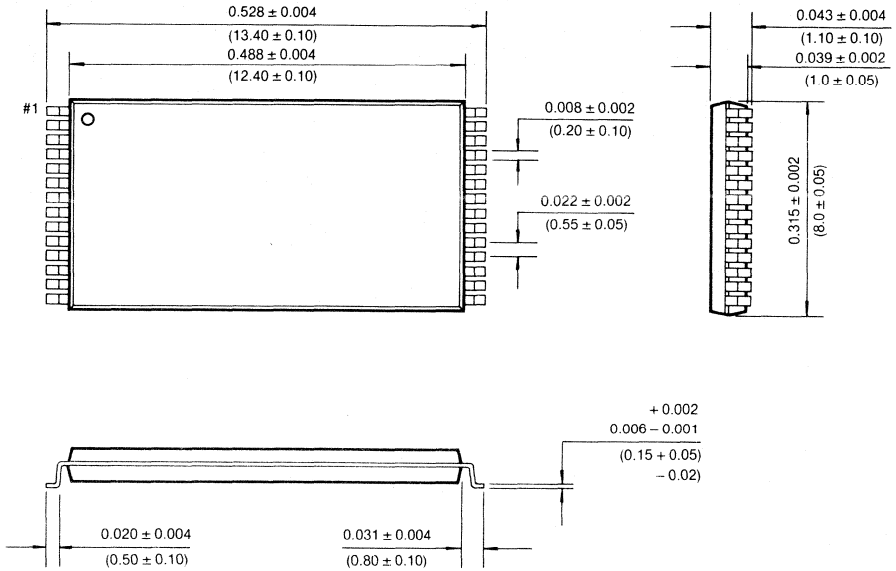
Unit: Inches (millimeters)



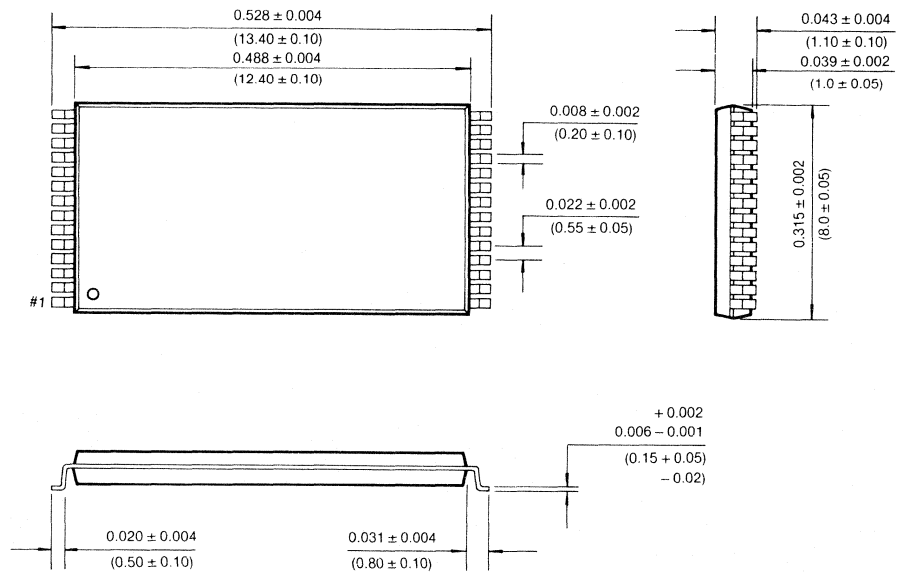
32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0814R)



28 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0813.4F)



28 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0813.4R)



65,536 WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time 55, 70, 85, 100ns (max.)**
- **Low Power Dissipation**
  - **Standby (CMOS): 10μW (typ.) L-Version**
  - **5μW (typ.) LL-Version**
  - **Operating : 35mW (typ.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (Min.)**
- **Standard Pin Configuration**
  - **KM68512LG/LG-L: 32-pin SOP (525mil)**
  - **KM68512LT/LT-L: 32-pin TSOP (Standard)**

GENERAL DESCRIPTION

The KM68512L/L-L is a 524,288-bit high-speed Static Random Access Memory organized as 65,536 words by 8 bits.

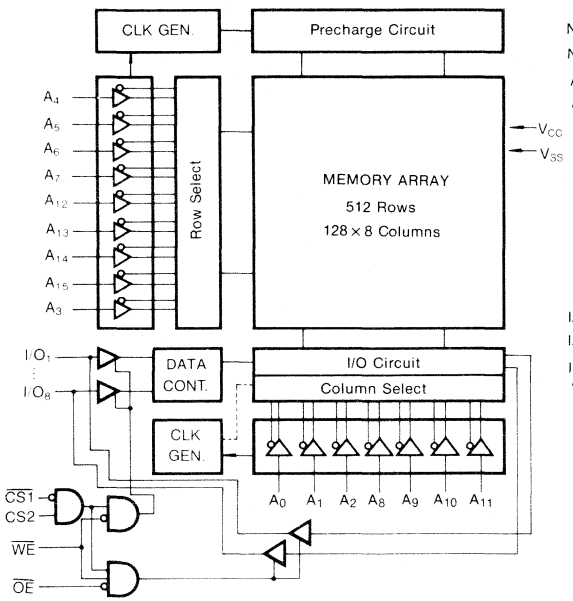
The KM68512L/L-L uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

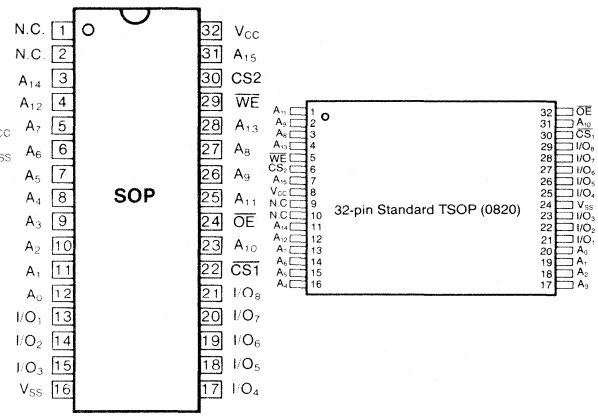
The KM68512L/L-L is particularly well suited for use in high-density high-speed system and low power app-lications.

It is particularly well suited for battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤50 ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL} or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}		−1	—	1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1} = V_{IL}$, CS2 = V_{IH} $V_{IN} = V_{IL}$ or V_{IH}, $I_{I/O}$ = 0mA		—	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, 100% Duty $\overline{CS1} \leq 0.2V$, CS2 ≥ V_{CC} − 0.2V $I_{I/O}$ = 0mA, $V_{IL} \leq 0.2V$, $V_{IH} \geq V_{CC} - 0.2V$		—	—	10	mA
	I_{CC2}	Min Cycle, 100% Duty $I_{I/O}$ = 0mA, $\overline{CS1} = V_{IL}$, CS2 = V_{IH}		—	—	70	mA
Standby Power Current	I_{SB}	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL}		—	—	3	mA
	I_{SB1}	$\overline{CS1} \geq V_{CC} - 0.2V$, CS2 ≥ V_{CC} − 0.2V or CS2 ≤ 0.2V	L	—	2	100	μA
			LL	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

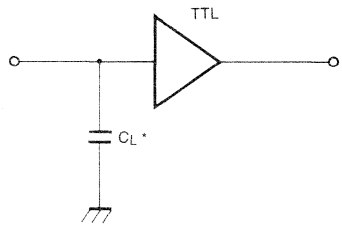
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 100^*pF + 1$ TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68512-5		KM68512-7		KM68512-8		KM68512-10		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		85		100		ns
Address Access Time	t_{AA}		55		70		85		100	ns
Chip Select to Output	t_{CO1}, t_{CO2}		55		70		85		100	ns
Output Enable to Output	t_{OE}		25		35		45		50	ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5	5	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	10		10		10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	0	30	0	30	ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	20	0	25	0	30	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		10		15		ns

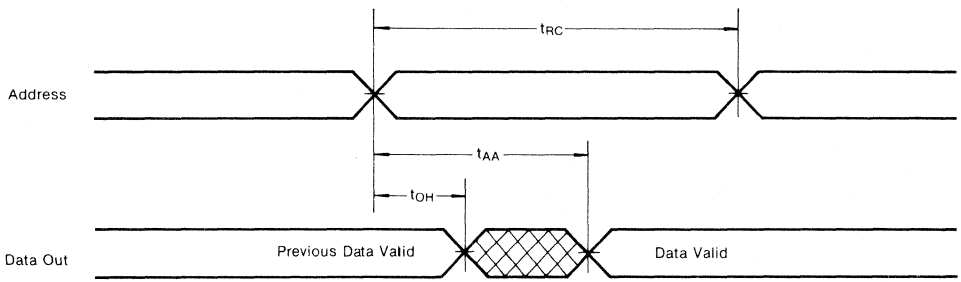
WRITE CYCLE

Parameter	Symbol	KM68512-5		KM68512-7		KM68512-8		KM68512-10		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		100		ns
Chip Select to End of Write	t_{CW}	45		60		70		80		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	50		60		70		80		ns
Write Pulse Width	t_{WP}	40		50		55		60		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	25		30		35		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		5		ns

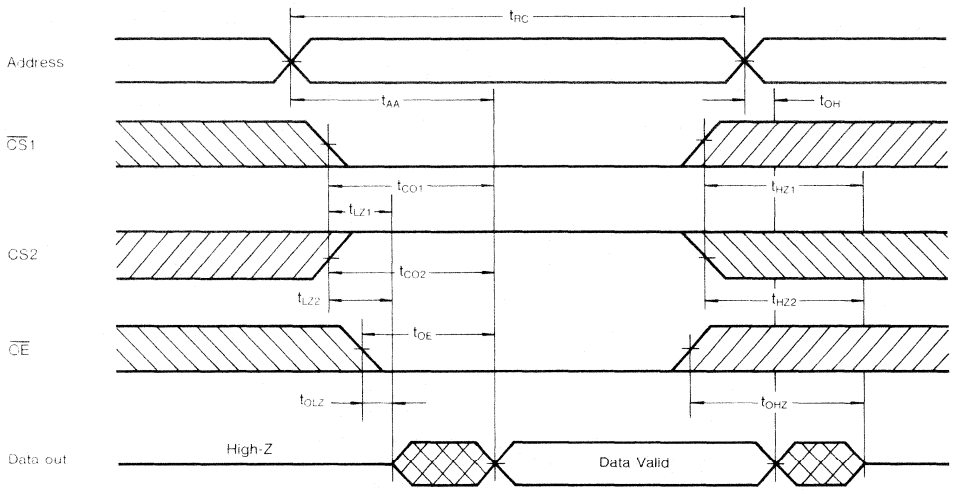
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = V_{IH}$, $\overline{WE} = V_{IH}$)



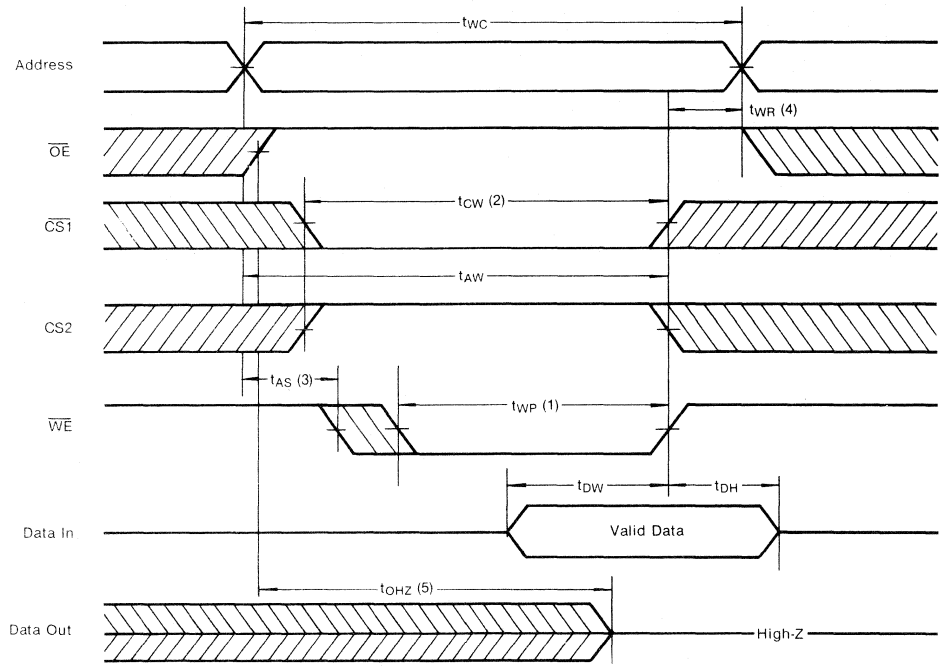
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



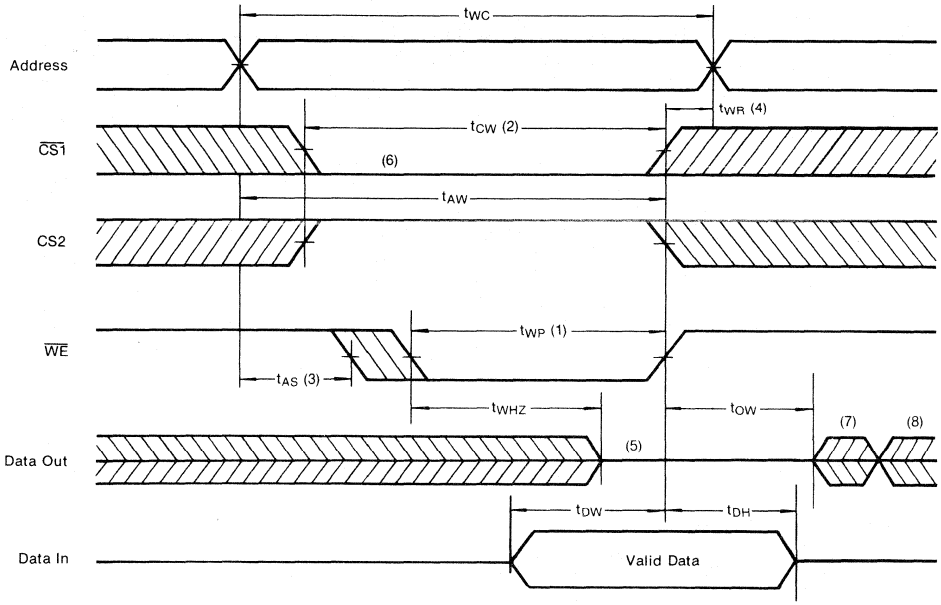
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ Low Fixed)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write end as $\overline{CS1}$, or $\overline{WE}$ going high, or CS2 going low.
5. During this period, I/O pins are in the output state, therefore, the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of next address.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

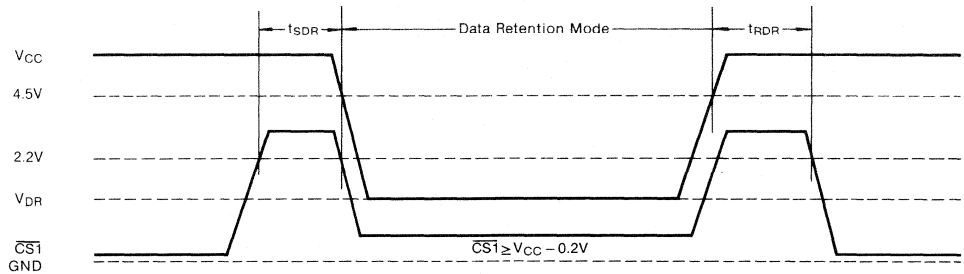
DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	CS1* ≥ V_{CC} − 0.2V		2.0	—	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V CS1 ≥ V_{CC} − 0.2V	L	—	1	50	μA
			LL	—	0.5	10	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0	—	—	ns
Recovery Time	t_{RDR}			t_{RC}**	—	—	ns

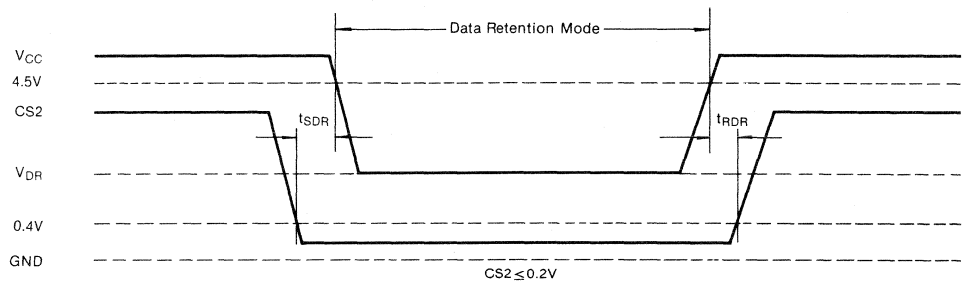
* : CS1 ≥ V_{CC} − 0.2, CS2 ≥ V_{CC} − 0.2 (CS1 Controlled) or CS2 ≤ 0.2 (CS2 Controlled)
** : Read Cycle Time

2

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



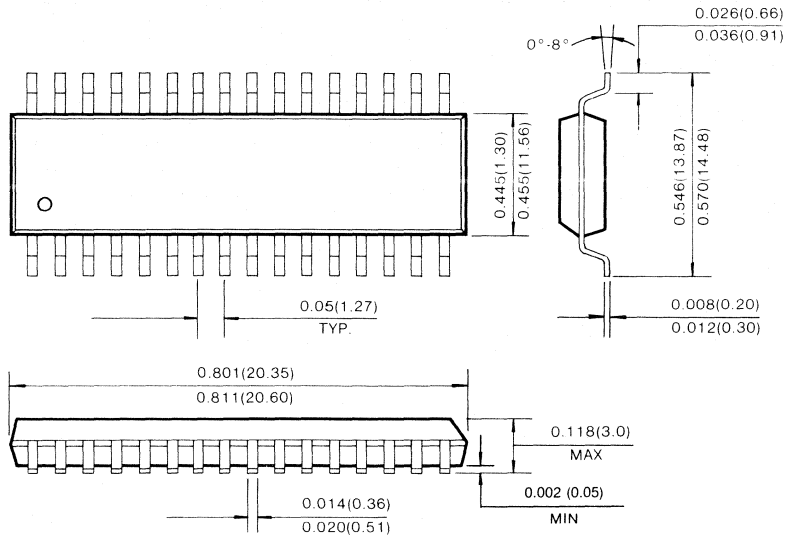
DATA RETENTION WAVEFORM (2) (CS2 Controlled)



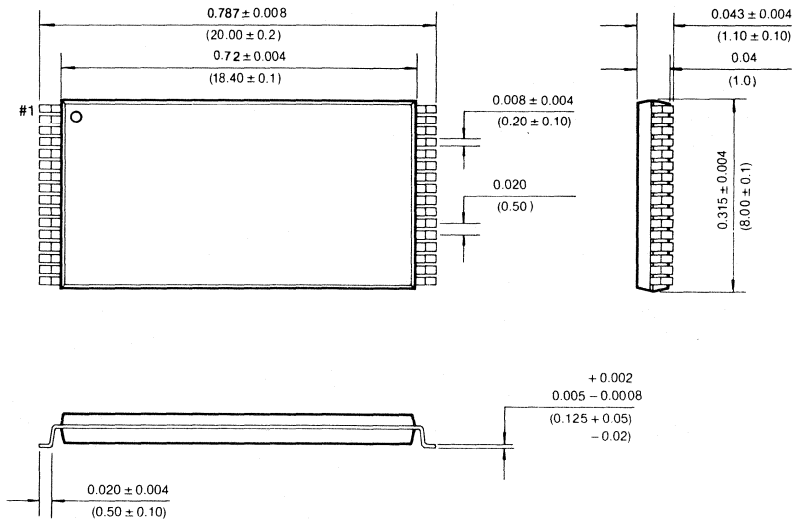
PACKAGE DIMENSIONS

32 PIN PLASTIC SMALL OUTLINE PACKAGE (525 mil)

Unit: Inches (millimeters)



32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0820F)



128K X 8 Bit CMOS Static RAM

FEATURES

- **Fast Access Time: 70, 85, 100, 120ns (max.)**
- **Low Power Dissipation**
  - **—Standby (CMOS): 10μW (typ.) L-Version**
    5μW(typ.) L-L Version
  - **—Operating: 110mW/MHz (max.)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Current:**
  50μA (max.)/L-Version
  10μA (max.)/L-L Version
- **Battery Back-up Operation**
  - **—2V (min.) Data Retention**
- **Standard Pin Configuration**
  KM681000LP/LP-L: 32 pin-DIP (600 mil)
  KM681000LG/LG-L: 32 pin-SOP (525 mil)

GENERAL DESCRIPTION

The KM681000L/L-L is a 1,048,576-bit high-speed Static random Access Memory organized as 131,072 words by 8 bits.

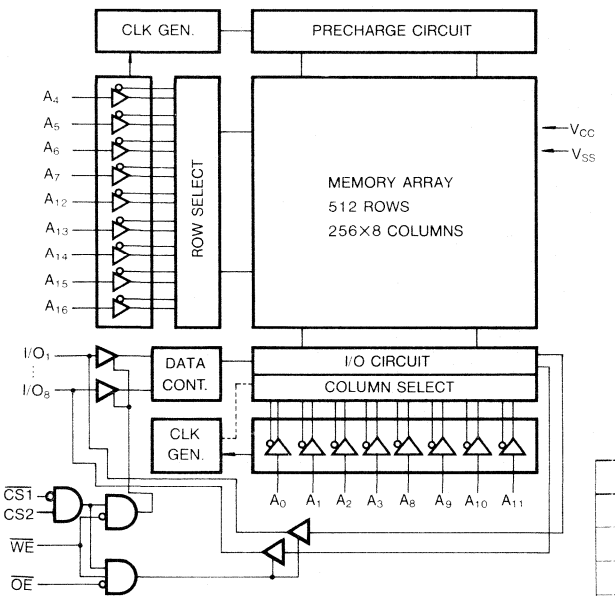
The device is fabricated using Samsung's advanced CMOS process.

The KM681000L/L-L has an output enable input for precise control of the data outputs.

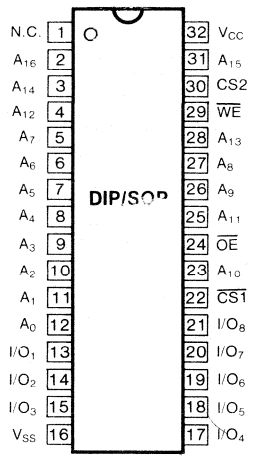
It also has chip select inputs for the minimum current power down mode.

The KM681000L/L-L has been designed for high speed and low power applications. It is particularly well suited for battery back-up nonvolatile memory applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Select
$\overline{OE}$	Output Enable
I/O1-I/O8	Data Inputs/Outputs
VCC	Power (+5V)
VSS	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ≤50ns pulse.

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		−1	—	+1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		−1	—	+1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA		—	—	25	mA
Average Operating Current	I_{CC1}	Cycle time=1μs, 100% Duty $\overline{CS1}$≤0.2V, CS2≥V_{CC}−0.2V $I_{I/O}$=0mA, V_{IL}≤0.2V, V_{IH}≥V_{CC}−0.2V		—	—	20	mA
	I_{CC2}	Min Cycle, 100% Duty $I_{I/O}$=0mA, $\overline{CS1}$=V_{IL}, CS2=V_{IH}		—	—	70	mA
Standby Power Supply Current	I_{sb}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}		—	—	3	mA
	I_{sb1}	$\overline{CS1}$≥V_{CC}−0.2V, CS2≥V_{CC}−0.2V or CS2≤0.2V	L	—	2	100	μA
			LL	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA		2.4	—	—	V

* Typ: V_{CC}=5V, T_A=25°C.

CAPACITANCE ($f=1MHz$, $T_A=25°C$)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0V$	—	8	pF

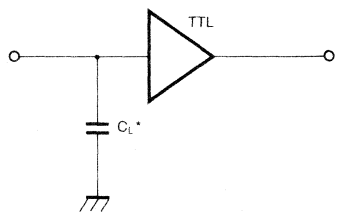
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITION ($T_A=0$ to $70°C$, $V_{CC}=5V\pm10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=100$ pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681000L-7 KM681000L-7L		KM681000L-8 KM681000L-8L		KM681000L-10 KM681000L-10L		KM681000L-12 KM681000L-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read CycleTime	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		85		100		120	ns
Output Enable to Valid Output	t_{OE}		35		45		50		60	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	10		10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	30	0	30	0	30	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	30	0	30	0	40	ns
Output Hold from Address Change	t_{OH}	10		10		15		15		ns

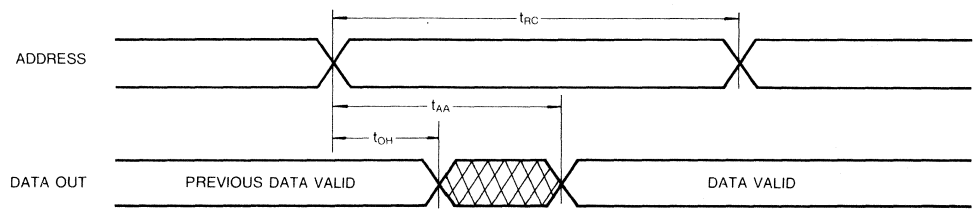
WRITE CYCLE

Parameter	Symbol	KM681000L-7 KM681000L-7L		KM681000L-8 KM681000L-8L		KM681000L-10 KM681000L-10L		KM681000L-12 KM681000L-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		70		80		85		ns
Address Set-Up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	60		70		80		85		ns
Write Pulse Width	t_{WP}	50		60		70		80		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		35		40		45		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
Edn Write to Output Low-Z	t_{OW}	5		5		5		5		ns

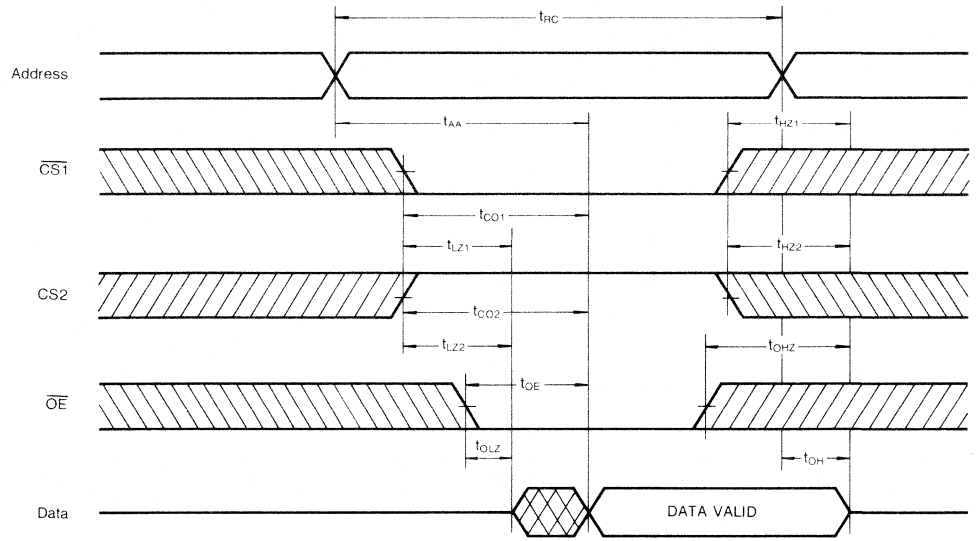
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=V_{IH}, $\overline{WE}$=V_{IH})



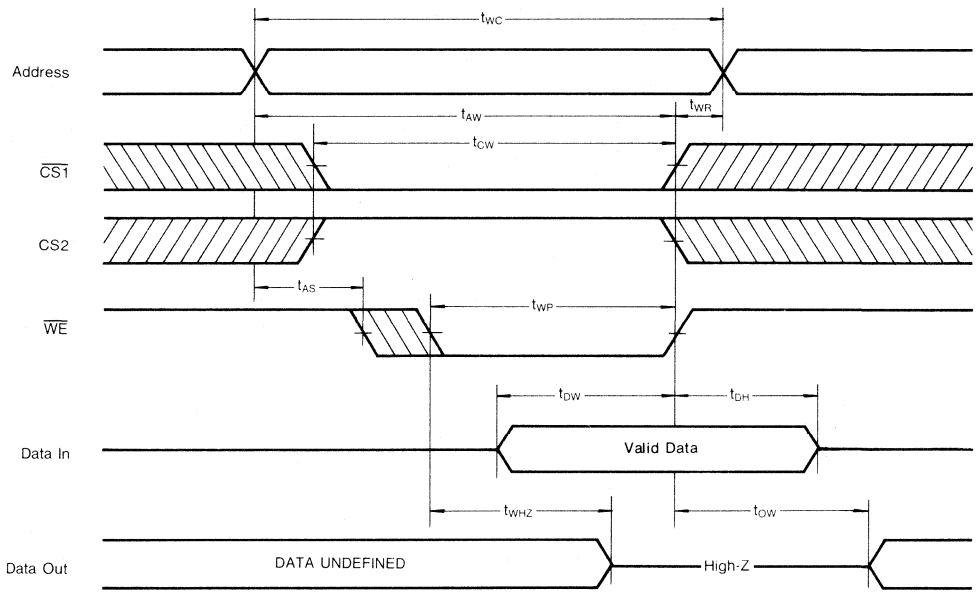
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$=V_{IH})



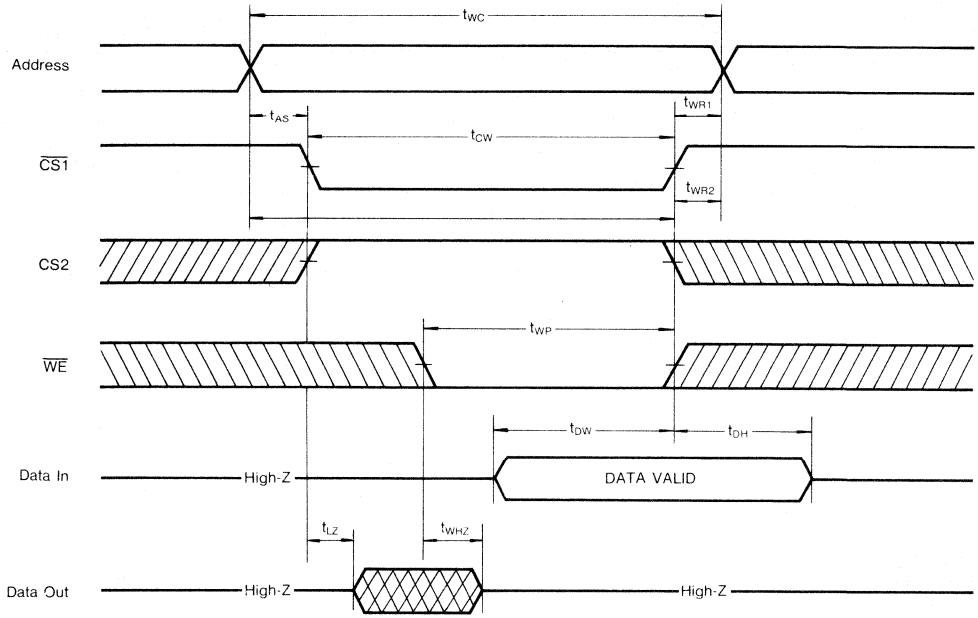
NOte (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.

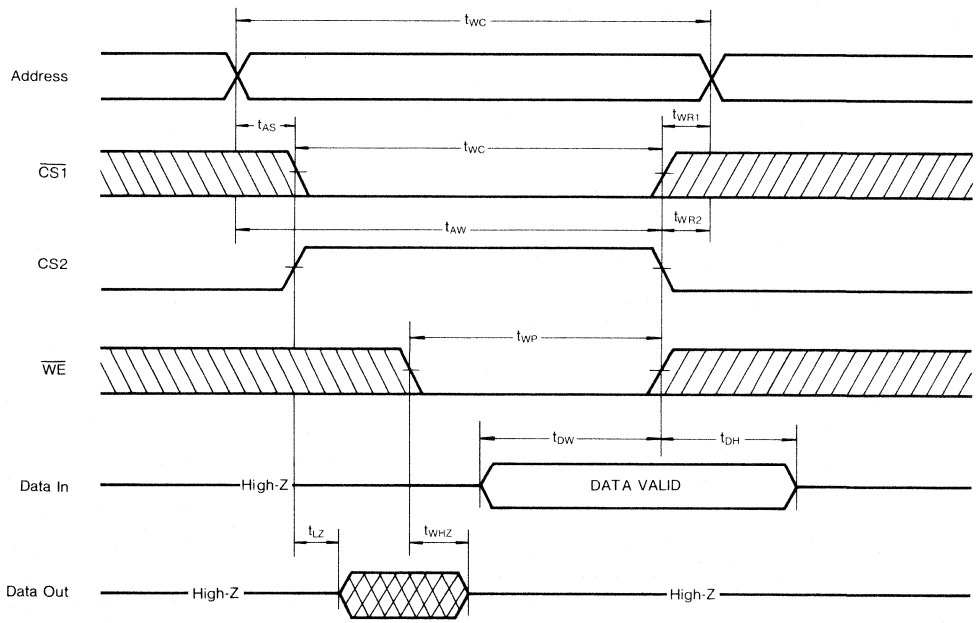
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2)($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (3)(CS2 Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$ and high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change, t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

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FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

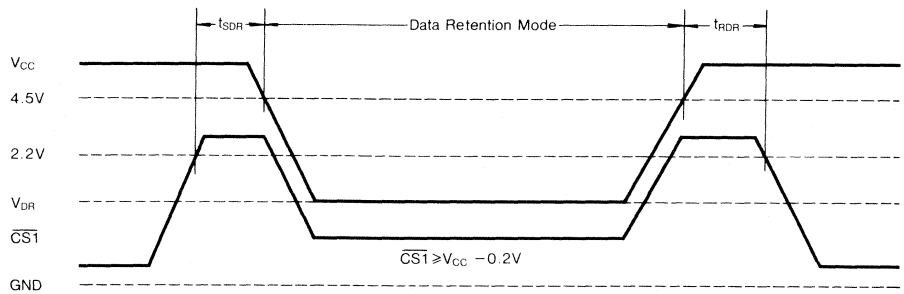
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

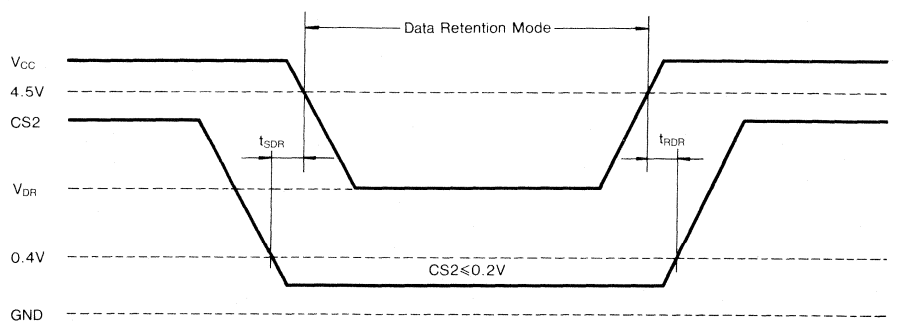
Parameter	Symbol	Test Conditions	Ver	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}-0.2V$ (1)	—	2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3V, $\overline{CS1} \geq V_{CC}-0.2V$ (1)	L	—	1.0	50 (2)	μA
			L-L	—	0.5	10 (3)	
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)	—	0	—	—	ns
Recovery Time	t_{RDR}			t_{RC} (4)	—	—	ns

(1) $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ ($\overline{CS1}$ Controlled) or $CS2 \leq 0.2V$ (CS2 Controlled)
(2) 20μA (max) at 0°C~40°C (Guaranteed only for L-version)
(3) 3μA (max) at 0°C~40°C (Guaranteed only for LL-version)
(4) t_{RC}=Read cycle time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



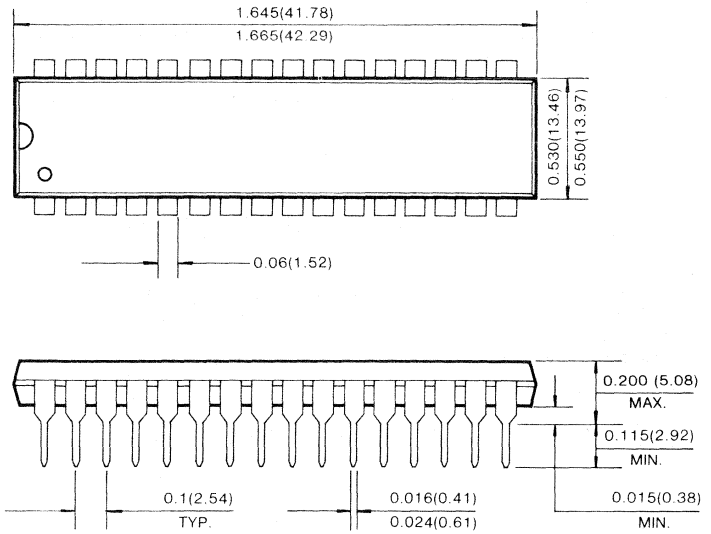
DATA RETENTION WAVEFORM (2) (CS2 Controlled)



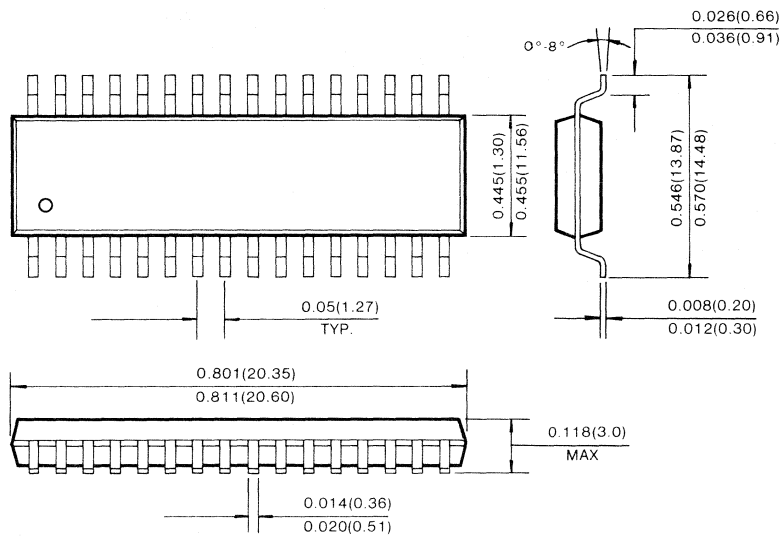
PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (Millimeters)



32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil)



128KX8 Bit Static RAM

FEATURES

- **Fast Access Time 70,85,100,120 ns (max.)**
- **Low Power Dissipation**
  - **Standby (CMOS): 10μW (typ.) L-Version**
  - **5μW (typ.) LL-Version**
  - **Operating : 35mW (typ.)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **— No clock or refresh required**
- **Three State Outputs**
- **Battery Back-up Operation**
  - **— 2V(min.) Data Retention**
- **Standard Pin Configuration**
  - **KM681000ALP/ALP-L : 32 pin-DIP (600mil)**
  - **KM681000ALG/ALG-L: 32 pin-SOP (525mil)**
  - **KM681000ALT/ALT-L : 32 pin-TSOP (Standard Type)**
  - **KM681000ALR/ALR-L: 32 pin-TSOP (Reverse Type)**

GENERAL DESCRIPTION

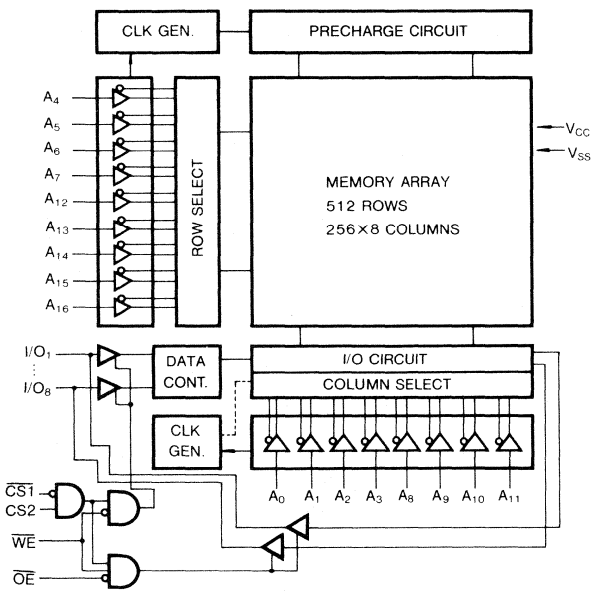
The KM681000AL/AL-L is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS process.

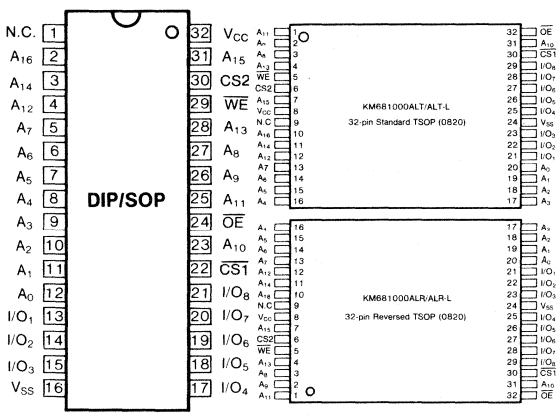
The KM681000AL/AL-L has an output enable input for precise control of the data outputs. It also has a chip enable input for the minimum current power down mode.

The KM681000AL/AL-L has been designed for high speed and low power applications. It is particularly well suited for battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Input/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_a	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min)=−3.0V for ⩽50ns pulse.

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		−1	—	+1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		−1	—	+1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, CS2=V_{IH} V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA		—	7	15	mA
Average Operating Current	I_{CC1}	Cycle time=1μs, 100% Duty $\overline{CS1}$⩽0.2V, CS2⩾V_{CC}−0.2V $I_{I/O}$=0mA, V_{IL}⩽0.2V, V_{IH}⩾V_{CC}−0.2V		—	—	10	mA
	I_{CC2}	Min Cycle, 100% Duty $I_{I/O}$=0mA, $\overline{CS1}$=V_{IL}, CS2=V_{IH}		—	—	70	mA
Standby Power Supply Current	I_{sb}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}		—	—	3	mA
	I_{sb1}	$\overline{CS1}$⩾V_{CC}−0.2V, CS2⩾V_{CC}−0.2V or CS2⩽0.2V	L	—	2	100	μA
			LL	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA		2.4	—	—	V

* Typ: V_{CC}=5V, T_A=25°C.

CAPACITANCE (f=1MHz, T_A=25°C)*

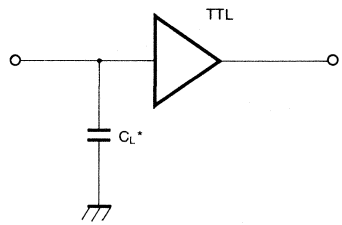
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

*Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=100pF+1TTL

TEST CIRCUIT



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681000AL-7 KM681000AL-7L		KM681000AL-8 KM681000AL-8L		KM681000AL-10 KM681000AL-10L		KM681000AL-12 KM681000AL-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		85		100		120	ns
Output Enable to Valid Output	t_{OE}		35		45		50		60	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	10		10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	25	0	30	0	30	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	0	30	0	40	ns
Output Hold from Address Change	t_{OH}	10		10		10		10		ns

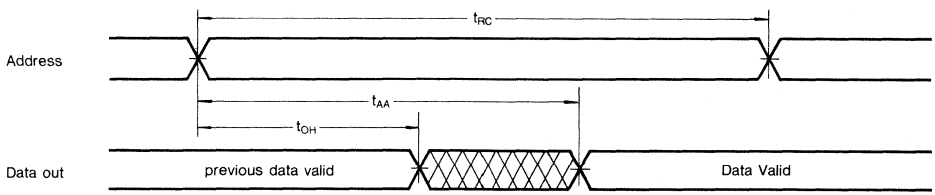
WRITE CYCLE

Parameter	Symbol	KM681000AL-7 KM681000AL-7L		KM681000AL-8 KM681000AL-8L		KM681000AL-10 KM681000AL-10L		KM681000AL-12 KM681000AL-12L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		70		80		85		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	60		70		80		85		ns
Write Pluse Width	t_{WP}	50		55		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		35		40		45		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		5		ns

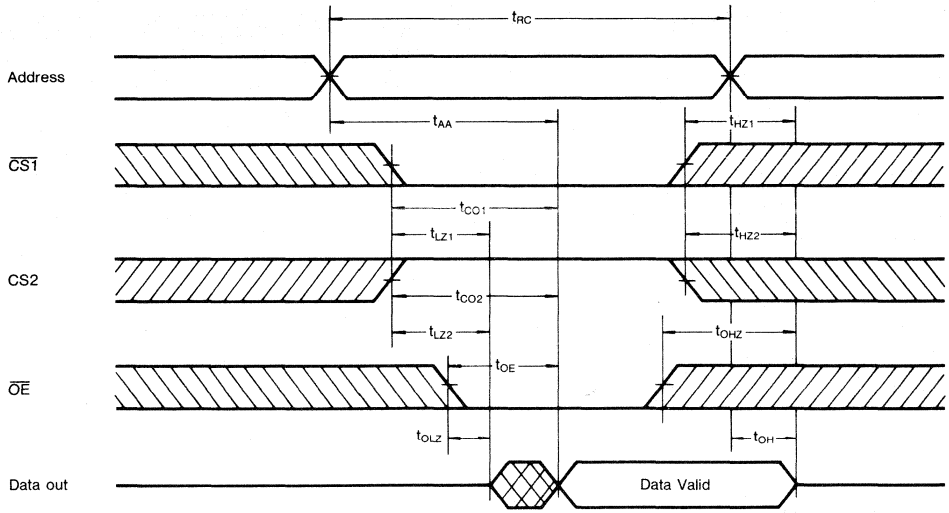
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=V_{IH}, $\overline{WE}$=V_{IH})



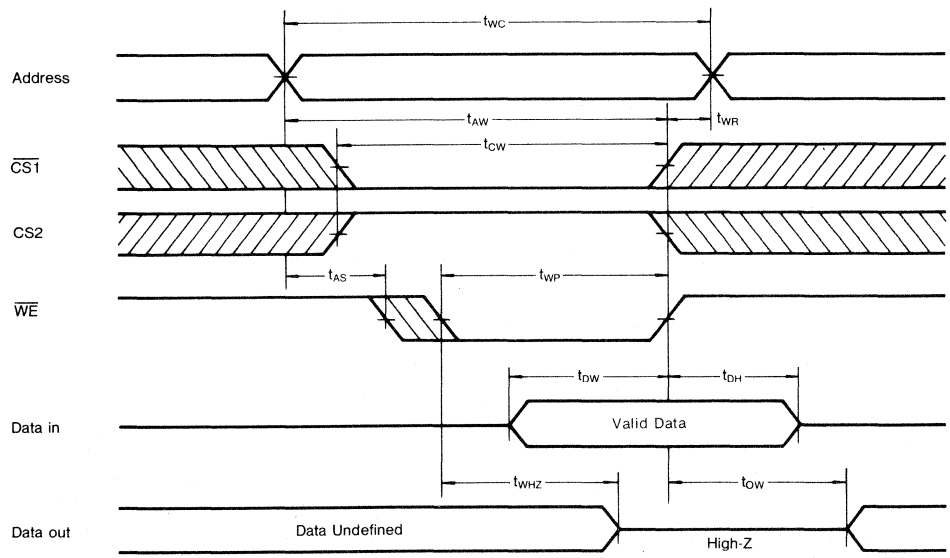
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



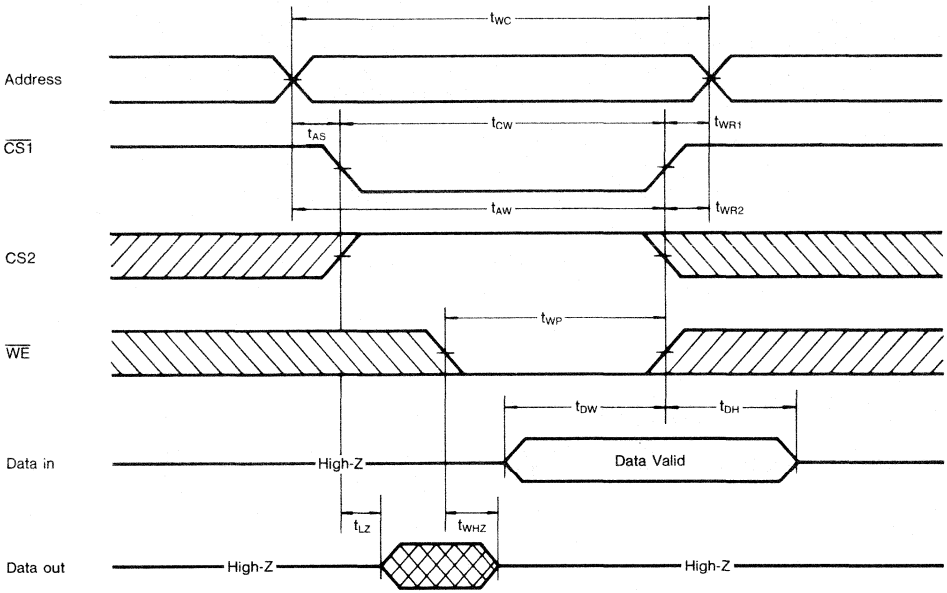
Note (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.

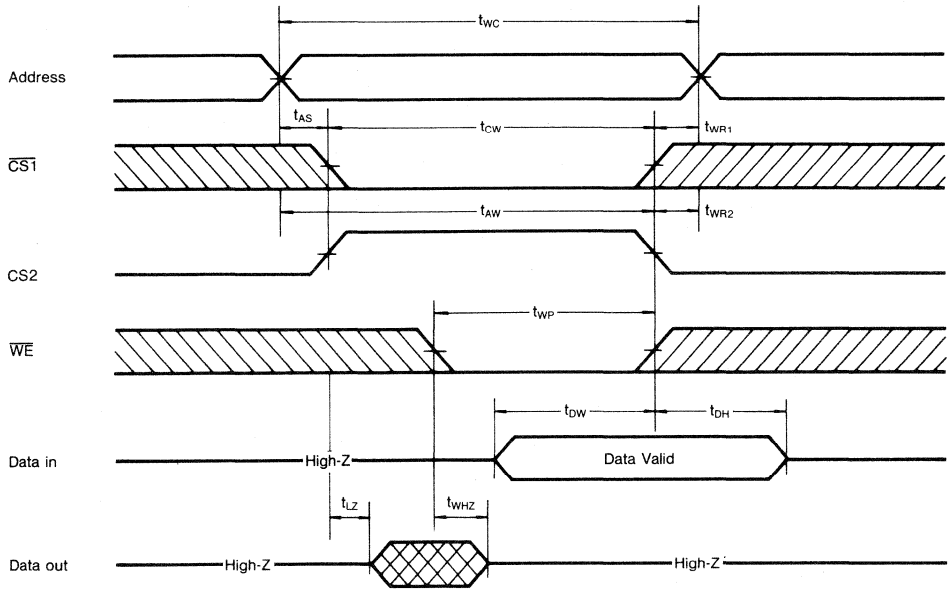
TIMING WAVEFORM OF WRITE CYCLE (1)($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (3) (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state, Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Power down	High-Z	I_{SB}, I_{SBI}
X	L	X	X	Power down	High-Z	I_{SB}, I_{SBI}
L	H	H	H	Output disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* X means don't care

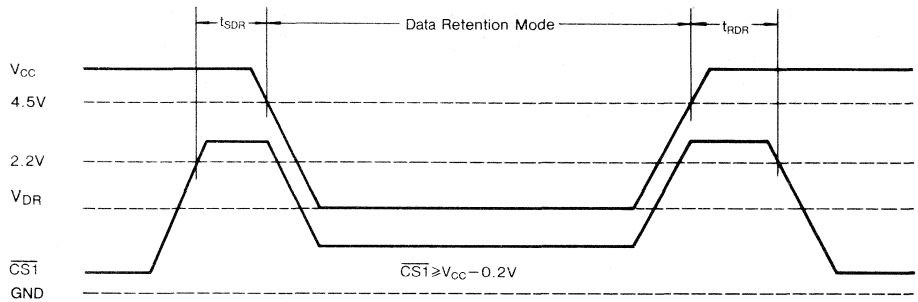
DATA RETENTION CHARACTERISTICS (T_A=0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}-0.2V$[1]		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC}=3V $\overline{CS1} \geq V_{CC}-0.2V$[1]	L		1.0	50[2]	μA
			LL		0.5	10[3]	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}[4]			ns

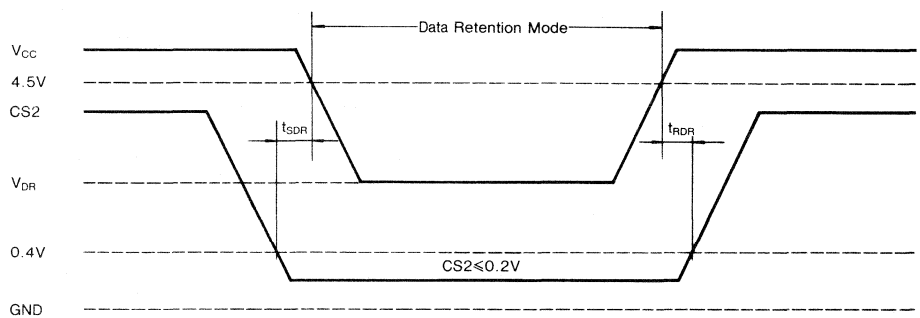
1) $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ ($\overline{CS1}$ Controlled) or $CS2 \leq 0.2V$ (CS2 Controlled)
2) 20μA (max.) at 0°C-40°C (Guaranteed only for L-version)
3) 3μA (max.) at 0°C-40°C (Guaranteed only for LL-version)
4) t_{RC}=Read cycle time

2

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



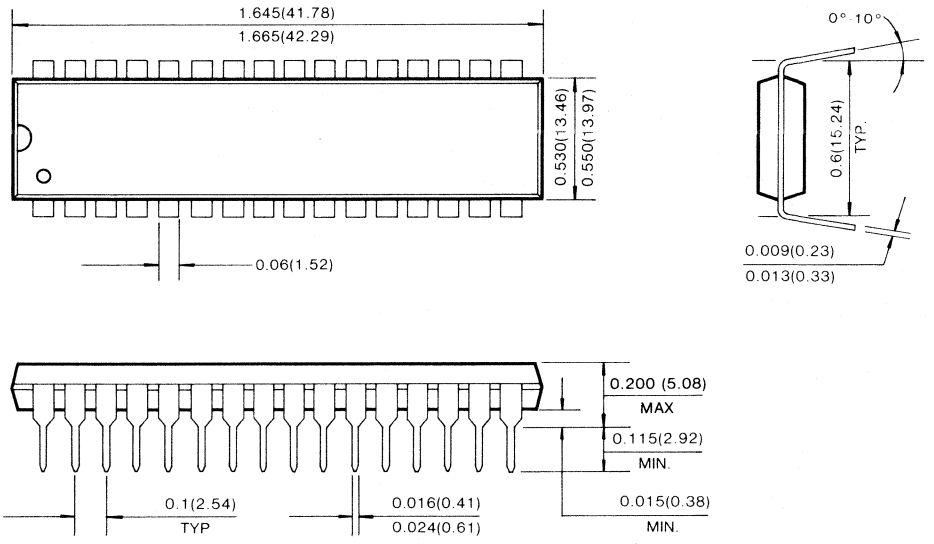
DATA RETENTION WAVEFORM (2) (CS2 Controlled)



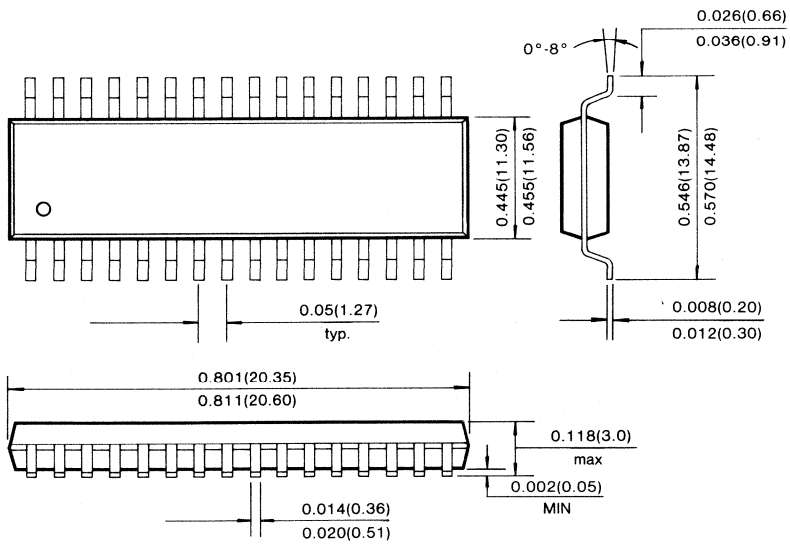
PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (Millimeters)



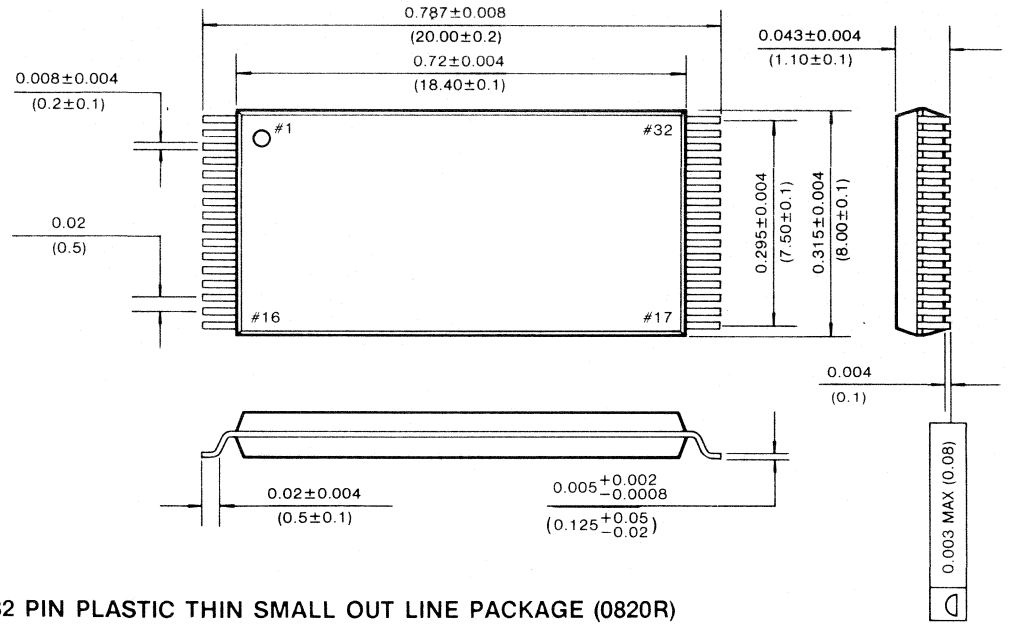
32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil)



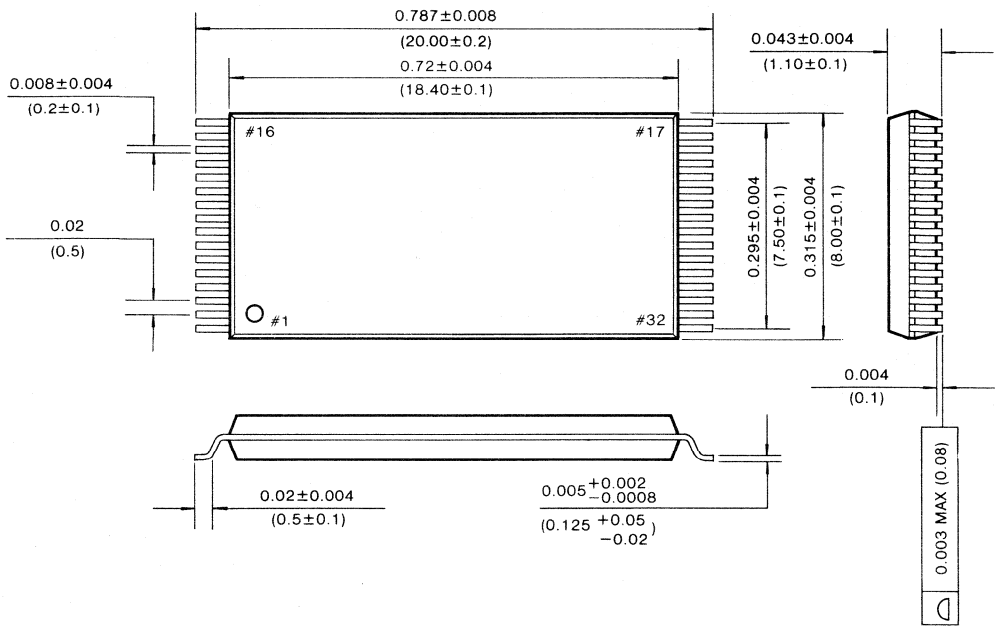
PACKAGE DIMENSIONS (Continued)

Unit: Inches (Millimeters)

32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0820F)



32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0820R)



131,072 WORD×8 Bit CMOS Static RAM

FEATURES

- **Industrial Temperature Range: – 40 to 85°C**
- **Fast Access Time: 70, 100ns (Max.)**
- **Low Power Dissipation**
  - **Standby (CMOS): 550μW (Max.) L-Ver.**
  - **275μW (Max.) LL-Ver.**
  - **Operating : 110mW (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (Min.)**
- **JEDEC Standard Pin Configuration**
  - **KM681000ALPI/ALPI-L: 32-pin DIP (600mil)**
  - **KM681000ALGI/ALGI-L: 32-pin SOP (525mil)**

GENERAL DESCRIPTION

The KM681000ALI/ALI-L is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

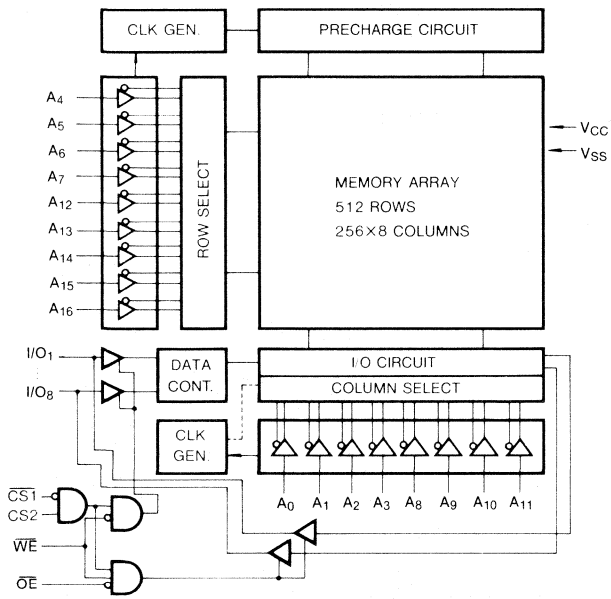
The device is fabricated using Samsung's advanced CMOS technology. The KM681000ALI/ALI-L has an output enable input for precise control of the data outputs.

It also has a chip enable input for the minimum current power down mode.

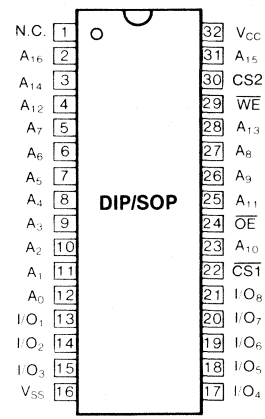
The KM68100ALI/ALI-L has been designed for high speed and low power application. It is particularly well suited for battery back-up memory application.

And – 40 to 85°C operating temperature range makes it ideal for industrial use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Selects
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	−40 to 85	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = −40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = −40 to 85°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL} or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}			−1	—	1	μA
Operation Power Supply Current	I_{CC}	$\overline{CS1} = V_{IL}$, CS2 = V_{IH}, $V_{IN} = V_{IL}$ or V_{IH}, $V_{I/O}$ = 0mA			—	7	20	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, 100% Duty, $\overline{CS1} \leq 0.2V$, CS2 ≥ V_{CC} − 0.2V, $I_{I/O}$ = 0mA, $V_{IL} \leq 0.2V$, $V_{IH} \geq V_{CC} - 0.2V$			—	—	15	mA
	I_{CC2}	Min. Cycle, 100% Duty $\overline{CS1} = V_{IL}$, CS2 = V_{IH}, $I_{I/O}$ = 0mA			—	—	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL}			—	—	3	mA
	I_{SB1}	$\overline{CS1} \geq V_{CC} - 0.2V$, CS2 ≥ V_{CC} − 0.2V or CS2 ≤ 0.2V	L Ver.	T_A = −40~85°C	—	2	100	μA
				T_A = 25°C	—	—	5	μA
			LL Ver.	T_A = −40~85°C	—	1	50	μA
				T_A = 25°C	—	—	2	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA			—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA			2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

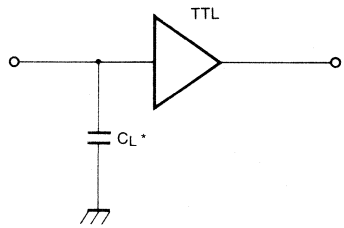
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 100pF + 1$ TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681000ALPI-7/7L KM681000ALGI-7/7L		KM681000ALPI-10/10L KM681000ALGI-10/10L		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO}		70		100	ns
Output Enable to Valid Output	t_{OE}		35		50	ns
Chip Select to Low-Z Output	t_{LZ1}, t_{LZ2}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	25	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		ns

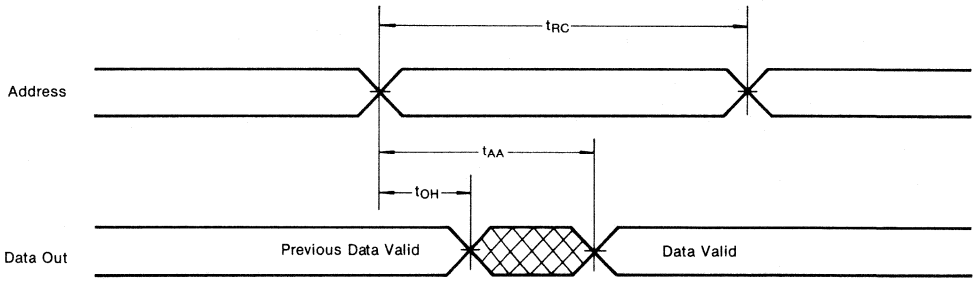
WRITE CYCLE

Parameter	Symbol	KM681000ALPI-7/7L KM681000ALGI-7/7L		KM681000ALPI-10/10L KM681000ALGI-10/10L		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		ns
Chip Select to End of Write	t_{CW}	60		80		ns
Address Valid to End of Write	t_{AW}	60		80		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	50		60		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	ns
Data to Write Time Overlap	t_{DW}	30		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	5		10		ns

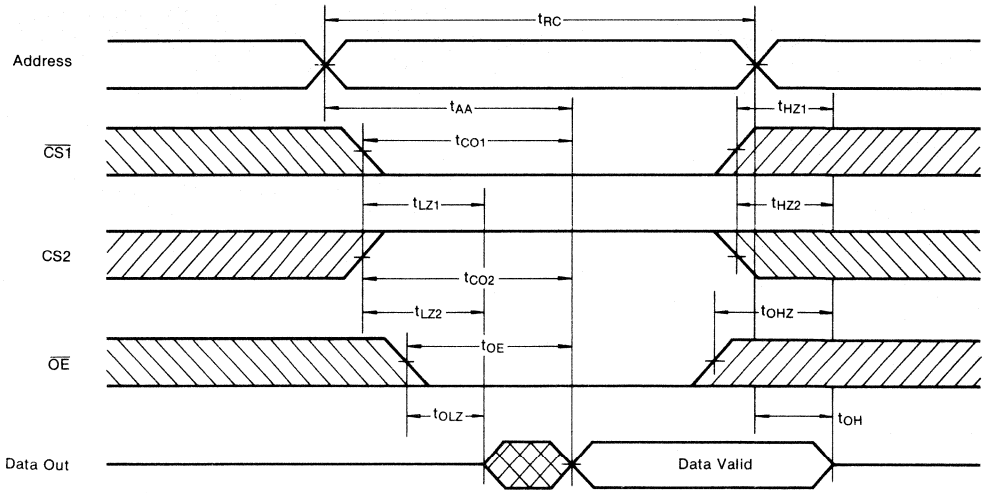
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = V_{IH}$, $\overline{WE} = V_{IH}$)



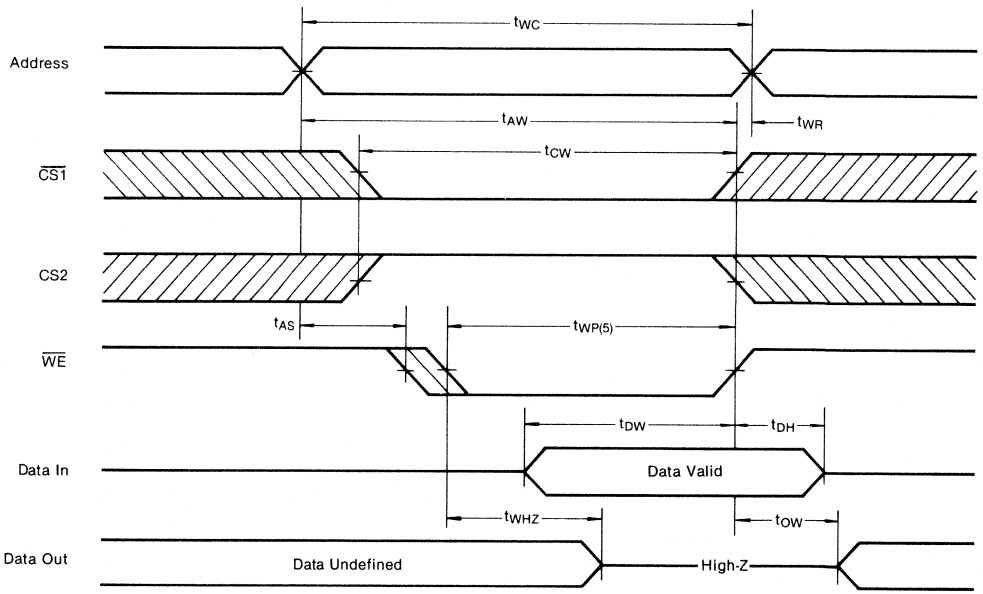
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



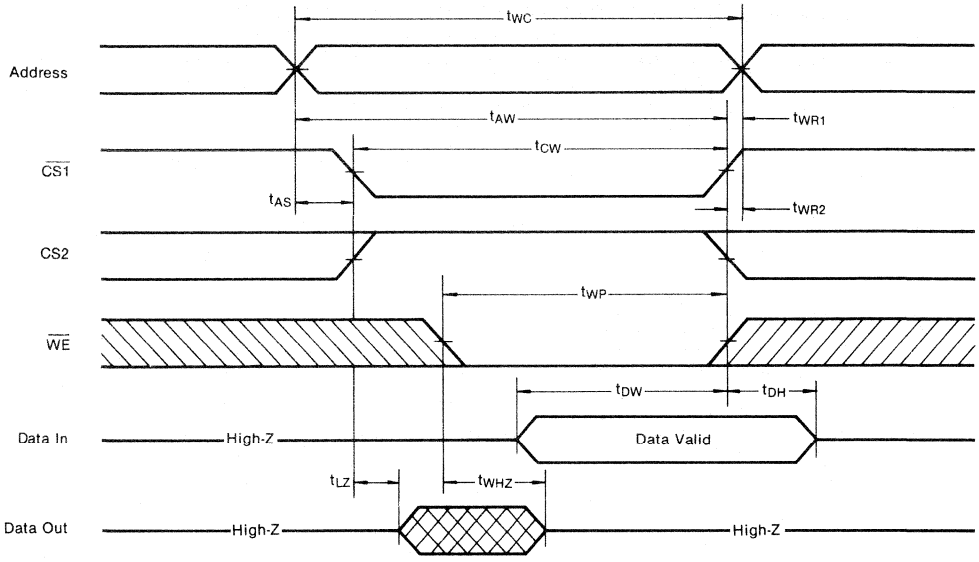
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

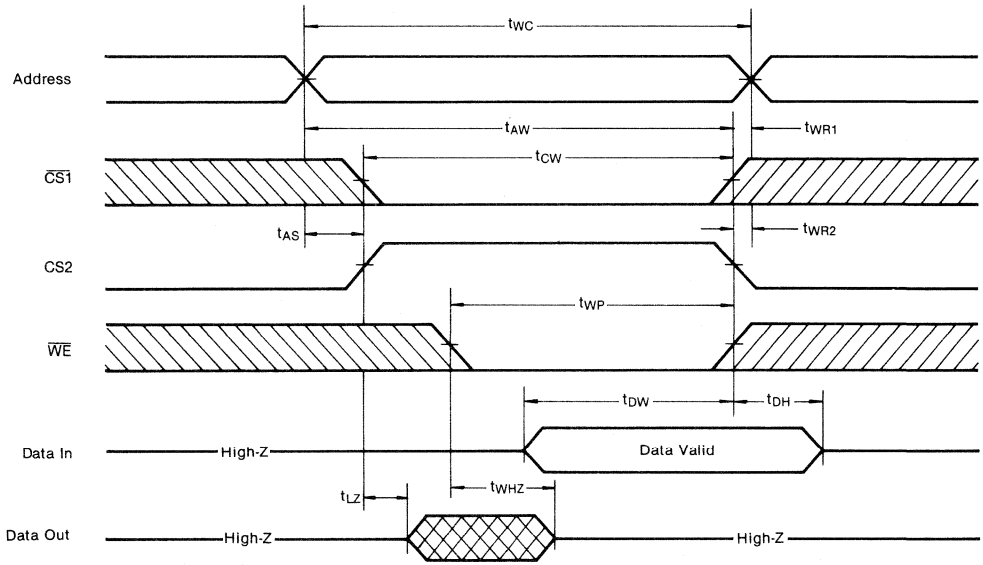
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (3) ($\overline{CS2}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and WE going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and WE going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* X means Don't Care.

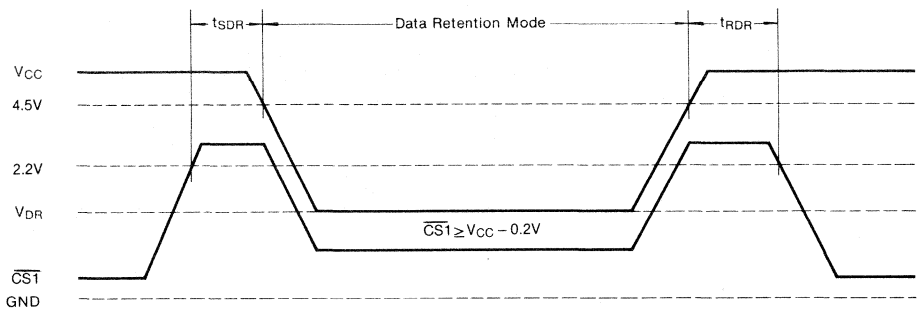
DATA RETENTION CHARACTERISTICS (T_A = −40 to 85°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}$* ≥ V_{CC} − 0.2V		2.0	—	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3V $\overline{CS1}$* ≥ V_{CC} − 0.2V	L-Ver.	—	1	50	μA
			LL-Ver.	—	0.5	20	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0	—	ns	
Recovery Time	t_{RDR}			t_{RC}**	—	—	ns

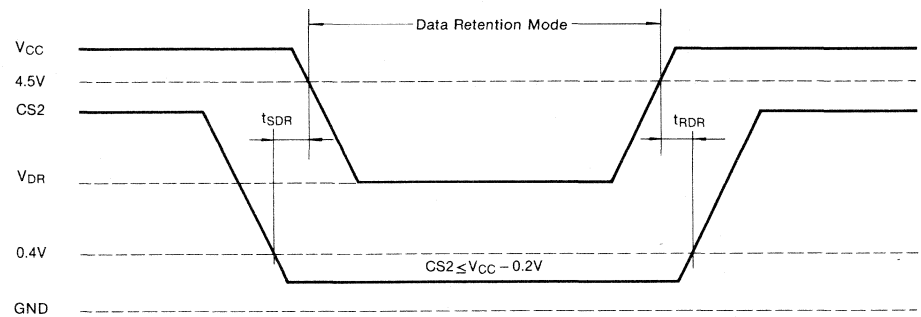
* $\overline{CS1}$ ≥ V_{CC} − 0.2, CS2 ≥ V_{CC} − 0.2 ($\overline{CS1}$ Controlled) or CS2 ≤ 0.2 (CS2 Controlled)
** Read Cycle Time

2

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



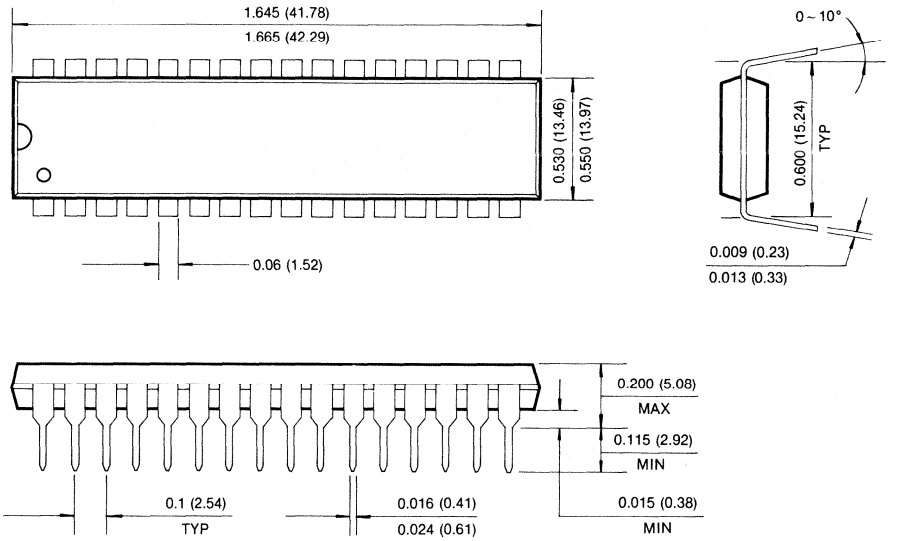
DATA RETENTION WAVEFORM (2) (CS2 Controlled)



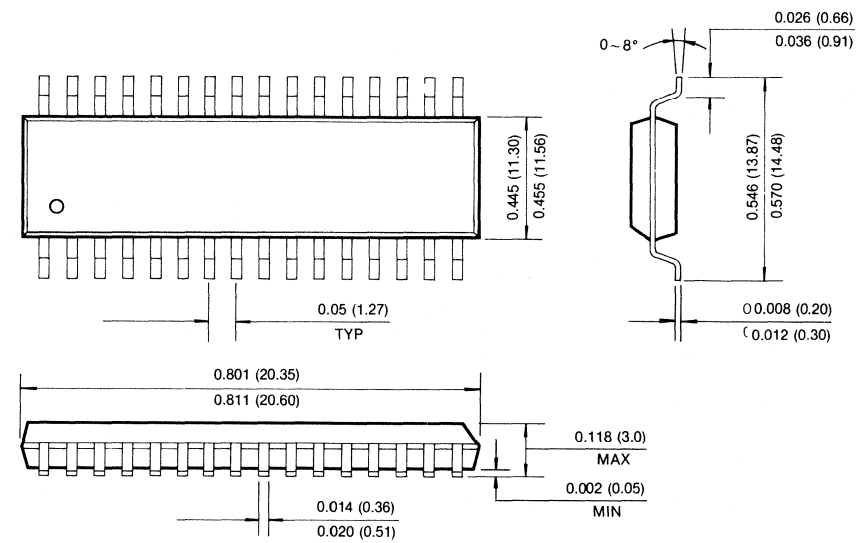
PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (millimeters)



32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil)



131,072 WORD×8 Bit CMOS Static RAM

FEATURES

- **Extended Operating Voltage: 2.7 ~ 5.5V**
- **Fast Access Time**
  - **3V Operation: 240ns (Max.)**
  - **5V Operation: 120ns (Max.)**
- **Low Power Dissipation Standby/Operating**
  - **3V Operation: 2.4μW/1.2mW (Typ.)**
  - **5V Operation: 5.0μW/35mW (Typ.)**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **JEDEC Standard Pin Configuration**
  - **KM681000ALP-V: 32-pin DIP (600mil)**
  - **KM681000ALG-V: 32-pin SOP (525mil)**
  - **KM681000ALT/R-V: 32-pin TSOP (Type-I)**

GENERAL DESCRIPTION

The KM681000AL-V is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

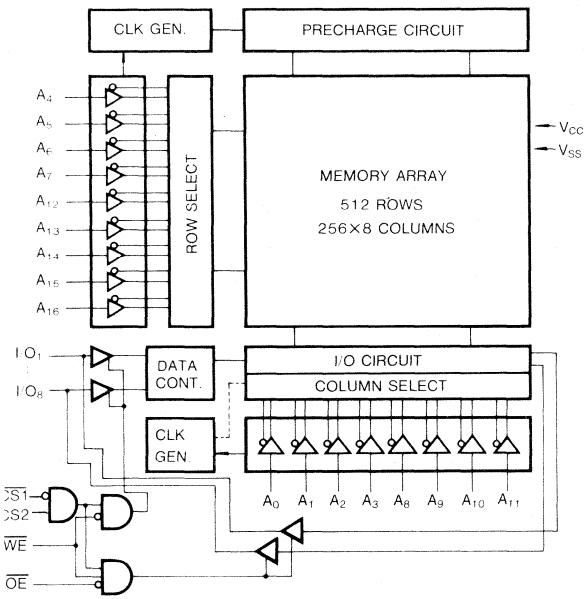
The device is fabricated using Samsung's advanced CMOS process and high-speed circuit technology.

The KM68100AL-V has an output enable input for precise control of the data outputs. It also has a chip enable inputs for the minimum current power down mode.

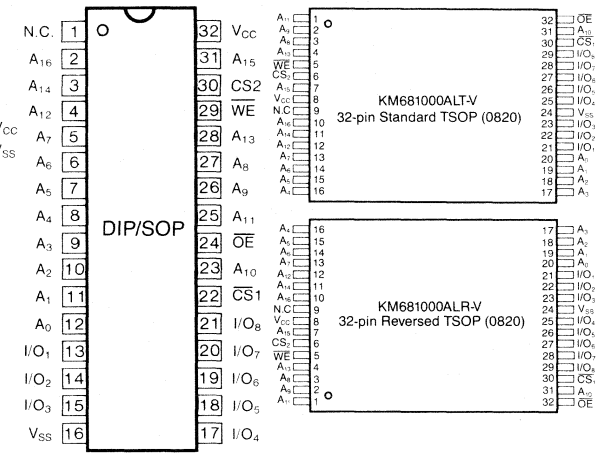
The KM68100AL-V is particulary well suited for use in low voltage (2.7 ~ 5.5V) operation and battery back-up applications.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Selects Inputs
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (2.7 ~ 5.5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to V_{CC} + 0.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.3*	—	0.4	V

* V_{IL}(min.) = −3.0V for ≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC} = 3V ± 10%			V_{CC} = 5V ± 10%			Unit
			Min	Typ*	Max	Min	Typ**	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}	−0.5	—	0.5	−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IL} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	−0.5	—	0.5	−1	—	1	μA
Operation Power Supply Current	I_{CC}	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IL} or V_{IH}, $V_{I/O}$ = 0mA	—	0.4	0.8	—	7	15	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, $\overline{CS1}$ ≤ 0.2V, CS2 ≥ V_{CC} − 0.2V, $I_{I/O}$ = 0mA, V_{IL} ≤ 0.2V, V_{IH} ≥ V_{CC} − 0.2V	—	2.5	5	—	—	10	mA
	I_{CC2}	Min. Cycle, 100% Duty $I_{I/O}$ = 0mA, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}	—	10	15	—	45	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	—	—	0.3	—	—	3	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{CC} − 0.2V, CS2 ≥ V_{CC} − 0.2V or CS2 ≤ 0.2V	—	0.8	20	—	1	50	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.2	—	—	2.4	—	—	V

* Typ: V_{CC} = 3V, T_A = 25°C
** Typ: V_{CC} = 5V, T_A = 25°C

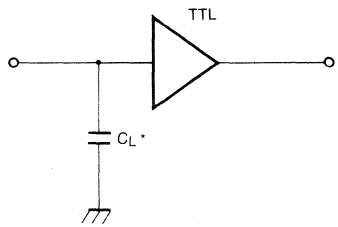
CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 3V \pm 10\%$, unless otherwise specified)

Parameter	Value	
	$V_{CC} = 3.0V$	$V_{CC} = 5.0V$
Input Pulse Level	2.2V/0.4V	2.4V/0.8V
Input Rise and Fall Time	5ns	5ns
Input and Output Timing Reference Levels	1.5V	1.5V
Output Load	$C_L = 100pF + 1$ TTL	$C_L = 100pF + 1$ TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	$V_{CC} = 3.0V \pm 10\%$		$V_{CC} = 5.0V \pm 10\%$		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	240		120		ns
Address Access Time	t_{AA}		240		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		240		120	ns
Output Enable to Valid Output	t_{OE}		120		60	ns
Chip Select to Low-Z Output	t_{LZ1}, t_{LZ2}	20		10		ns
Output Enable to Low-Z Output	t_{OLZ}	10		5		ns
Chip Disselect to High-Z Output	t_{HZ1}, t_{HZ2}	0	80	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	80	0	40	ns
Output Hold from Address Change	t_{OH}	30		10		ns

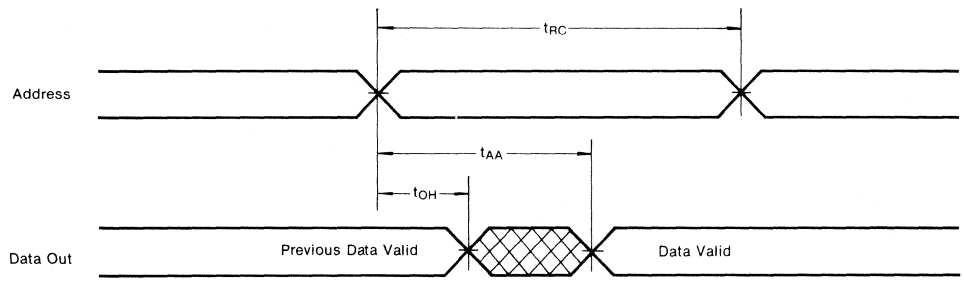
WRITE CYCLE

Parameter	Symbol	V_{CC} = 3.0V ± 10%		V_{CC} = 5.0V ± 10%		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	240		120		ns
Chip Select to End of Write	t_{CW}	170		85		ns
Address Valid to End of Write	t_{AW}	170		85		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	160		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	60	0	30	ns
Data to Write Time Overlap	t_{DW}	100		45		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	20		5		ns

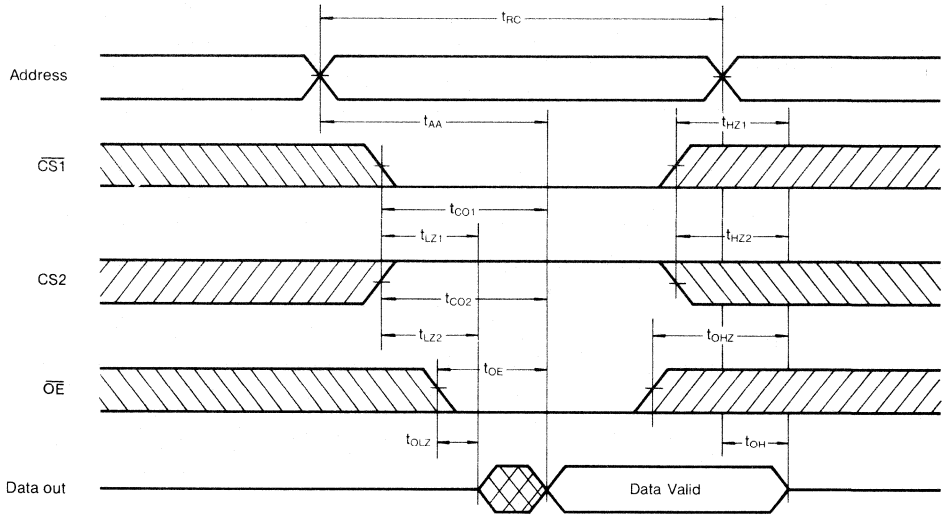
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = V_{IH}, $\overline{WE}$ = V_{IH})



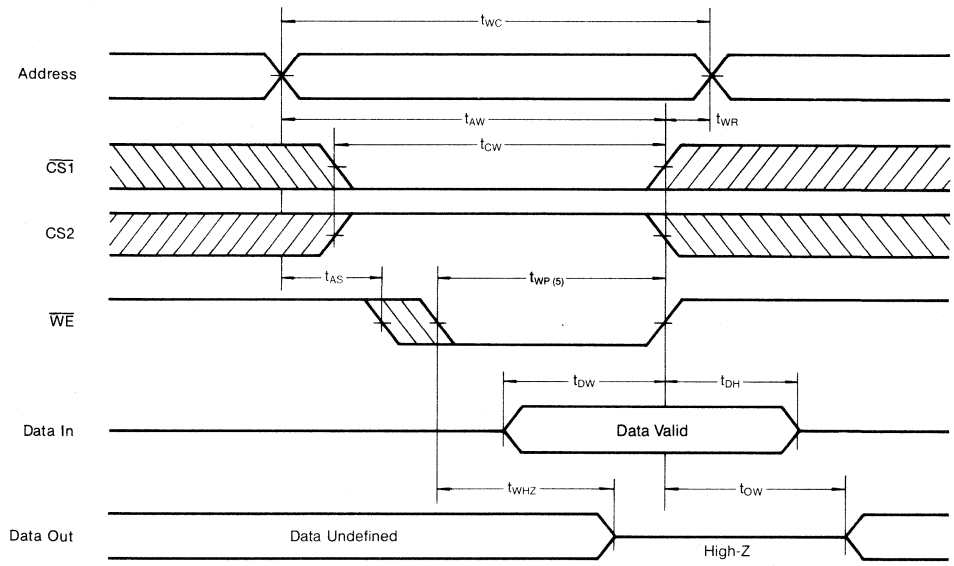
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



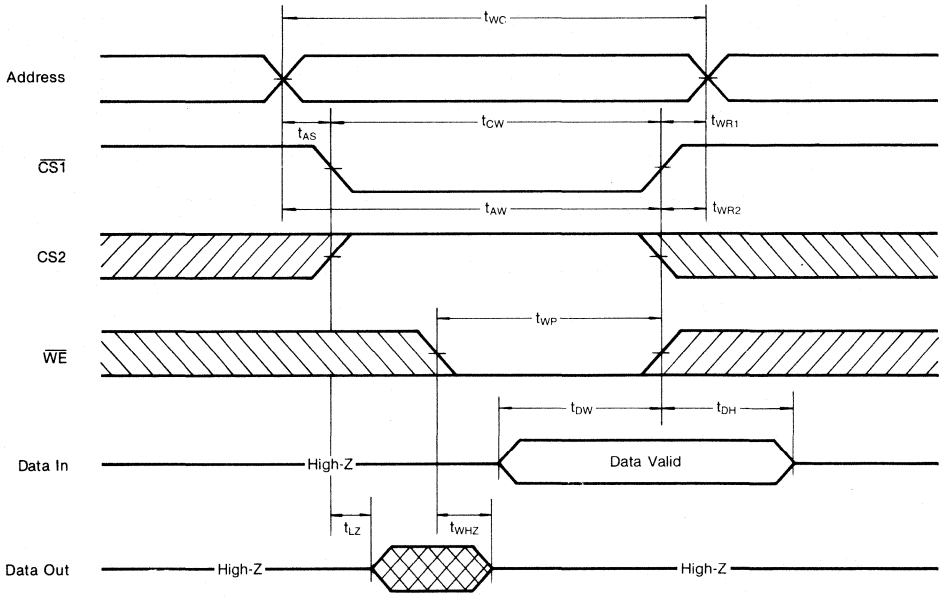
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

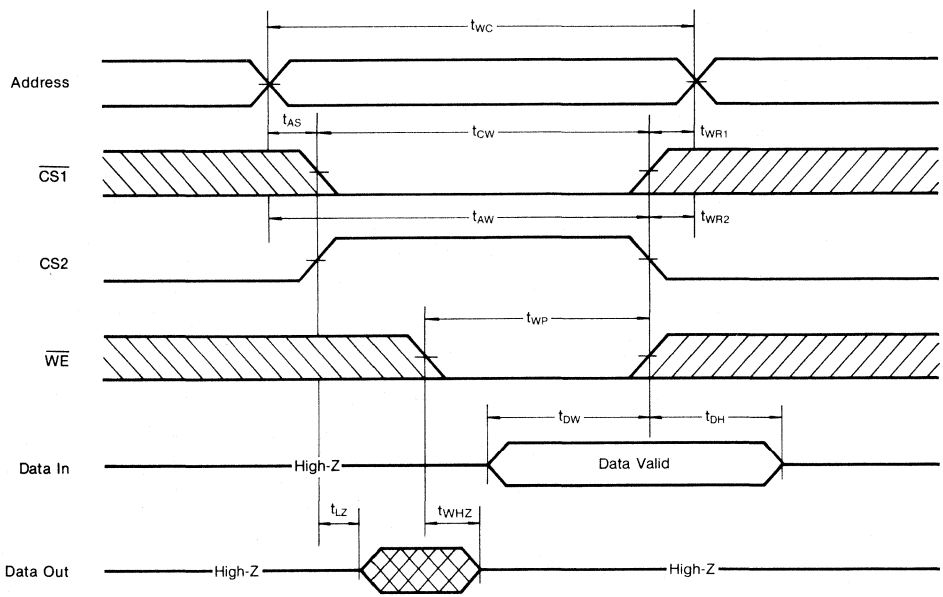
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (3) (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low WE. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

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FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

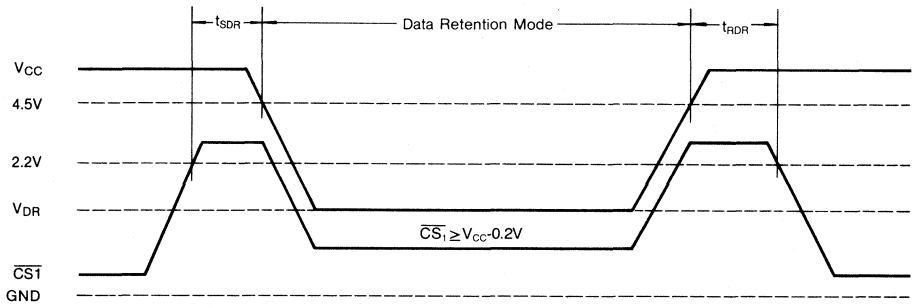
* X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

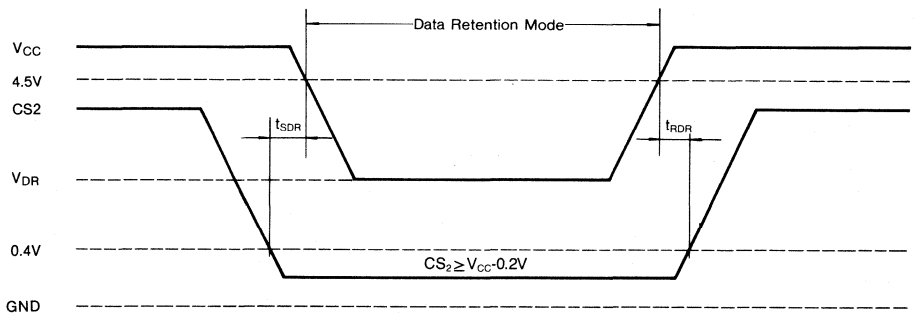
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}$* ≥ V_{CC} − 0.2V		2.0	—	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3V $\overline{CS1}$* ≥ V_{CC} − 0.2V	0~70°C	—	—	20	μA
			0~40°C	—	—	5	μA
			25°C	—	0.5	0.8	μA
		V_{CC} = 2.7~5.5V		—	1	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0	—	—	ns
Recovery Time	t_{RDR}			t_{RC}**	—	—	ns

* $\overline{CS1}$ ≥ V_{CC} − 0.2, CS2 ≥ V_{CC} − 0.2 ($\overline{CS1}$ Controlled) or CS2 ≤ 0.2 (CS2 Controlled)
** Read Cycle Time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



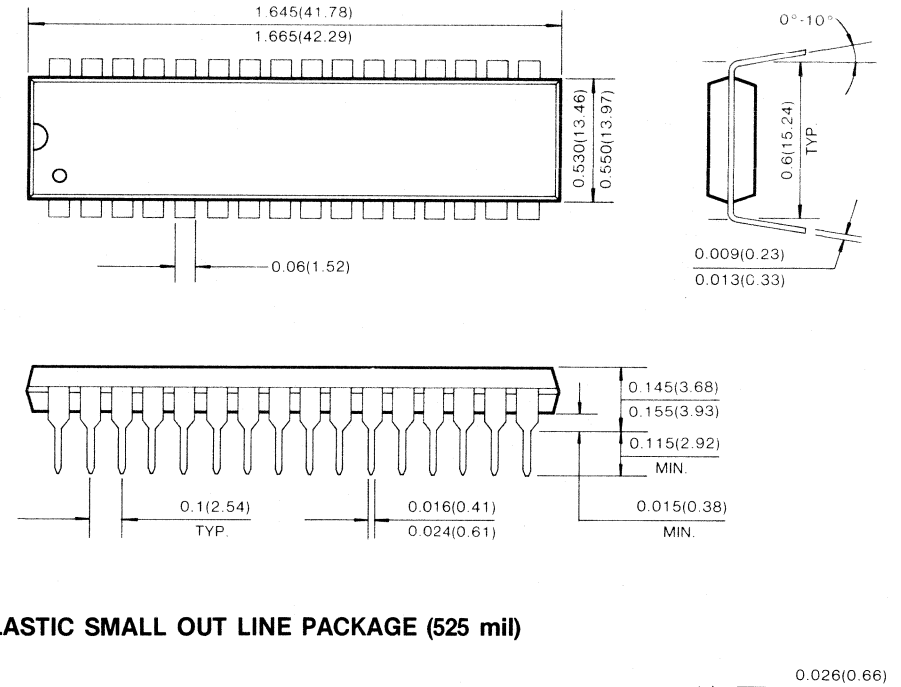
DATA RETENTION WAVEFORM (2) (CS2 Controlled)



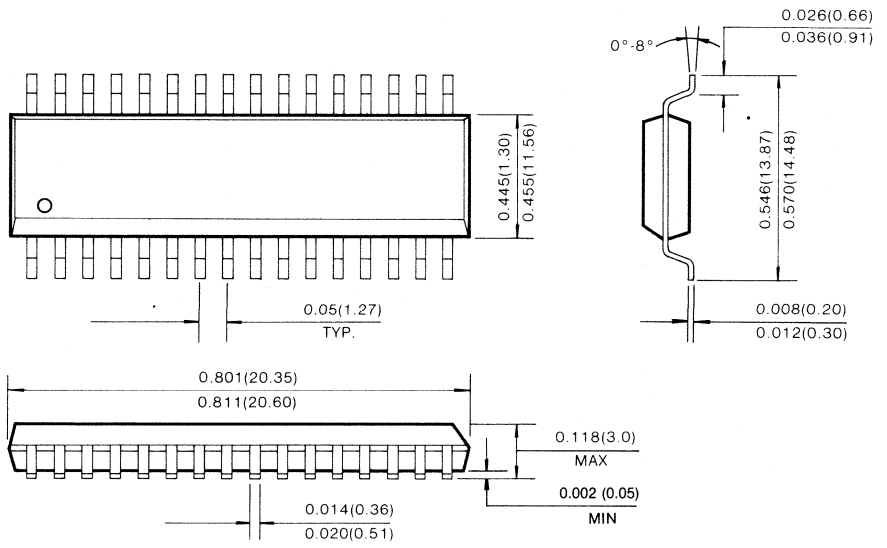
PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (millimeters)



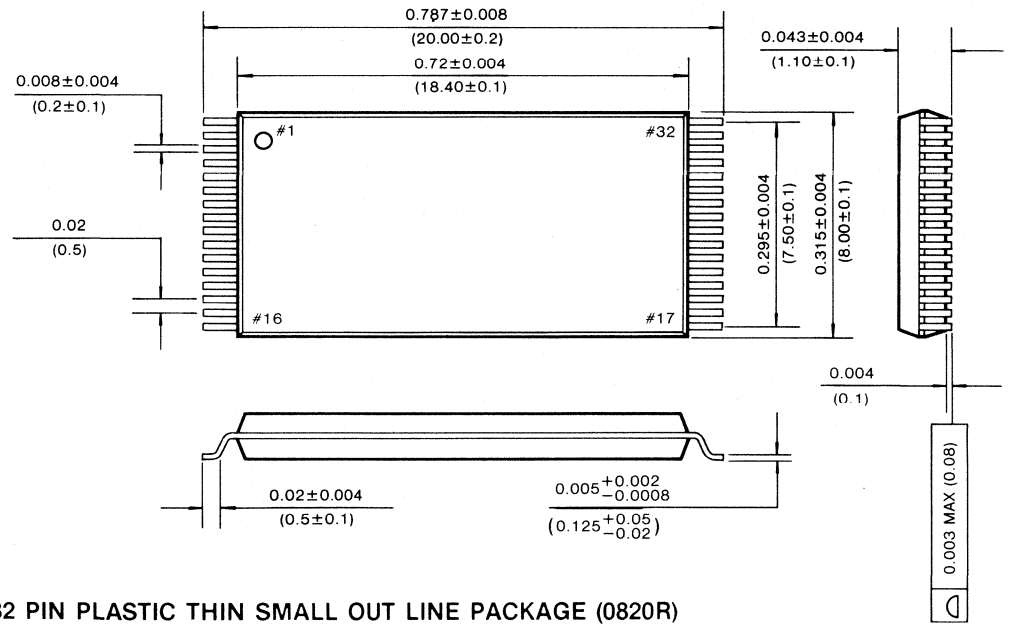
32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil)



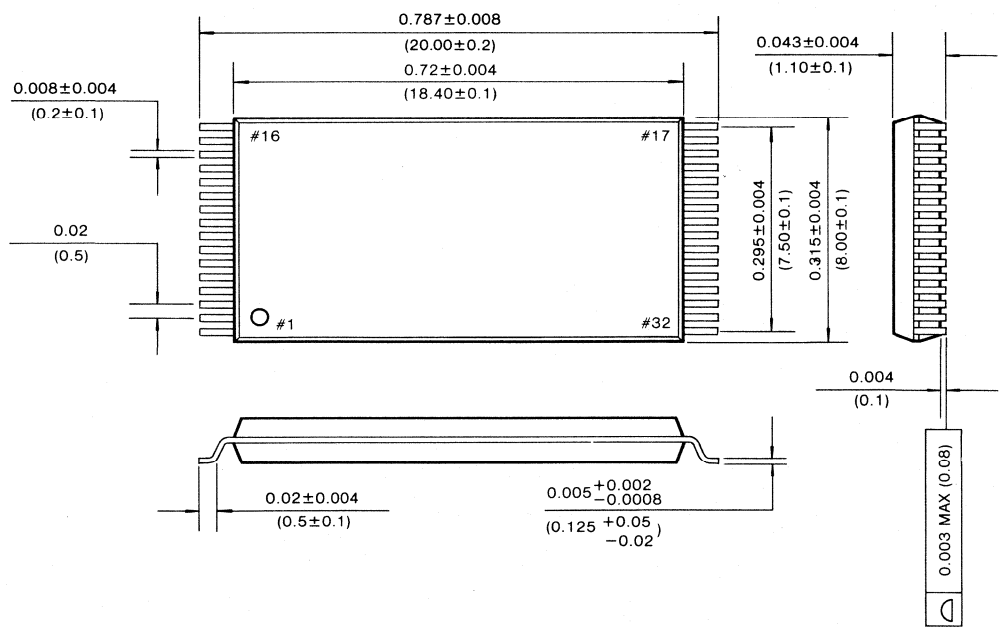
PACKAGE DIMENSIONS (Continued)

Unit: Inches (Millimeters)

32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0820F)



32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (0820R)



524,288 WORD×8 Bit CMOS Static RAM

FEATURES

- **Fast Access Time: 55, 70, 85, 100ns (Max.)**
- **Low Power Dissipation**
  Standby (CMOS): 10μW (Typ.) L Version
  5μW (Typ.) L-L Version
  Operating: 110mW/MHz (Max.)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Three State Outputs**
- **Battery Back-up Operation**
  2V (Min.) Data Retention
- **Standard Pin Configuration**
  KM684000LP/LP-L: 32-pin DIP (600mil)
  KM684000LG/LG-L: 32-pin SOP (525mil)
  KM684000LT/LT-L: 32-pin TSOP (400mil), Standard
  KM684000LR/LR-L: 32-pin TSOP (400mil), Reverse

GENERAL DESCRIPTION

The KM684000L/L-L is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS process.

The KM684000L/L-L has an output enable input for precise control of the data outputs.

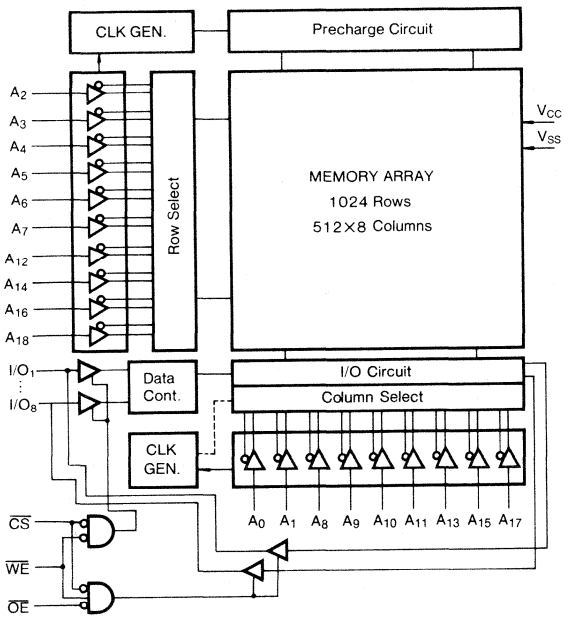
It also has a chip enable inputs for the minimum current power down mode.

The KM684000L/L-L has been designed for high speed and low power application.

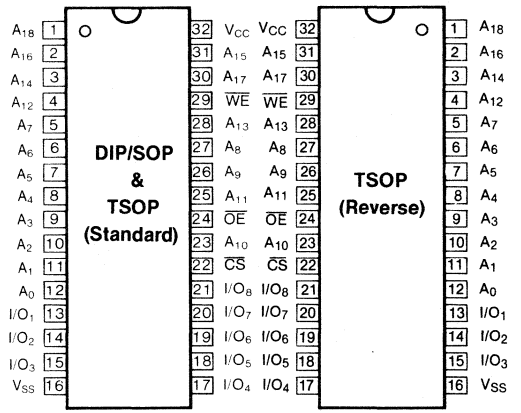
It is particularly well suited for battery back-up nonvolatile memory application.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top View)



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−55 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

* **V_{IL}(min) = −3.0V for** ≤50ns Pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		−1	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}		−1	—	1	μA
Operation Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}/V_{IH}$, $I_{I/O}$ = 0mA		—	—	25	mA
Average Operating Current	I_{CC1}	Cycle Time = 1μs, 100% Duty, $\overline{CS} \leq 0.2V$, $V_{IH} \geq V_{CC} - 0.2V$ $V_{IL} \leq 0.2V$, $I_{I/O}$ = 0mA		—	—	20	mA
	I_{CC2}	Min Cycle, 100% Duty, $\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}, $I_{I/O}$ = 0mA		—	—	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$		—	—	3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L	—	2	100	μA
			L-L	—	1	20	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

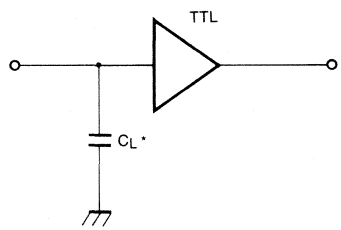
CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Loads	$C_L = 100*pF + 1$ TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM684000L-5 KM684000L-5L		KM684000L-7 KM684000L-7L		KM684000L-8 KM684000L-8L		KM684000L-10 KM684000L-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		85		100		ns
Address Access Time	t_{AA}		55		70		85		100	ns
Chip Select to Output	t_{CO}		55		70		85		100	ns
Output Enable to Valid Output	t_{OE}		25		35		45		50	ns
Chip Select to Low-Z Output	t_{LZ}	10		10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		5		ns
Chip Disselect to High-Z Output	t_{HZ}	0	20	0	25	0	30	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	0	30	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		10		15		ns

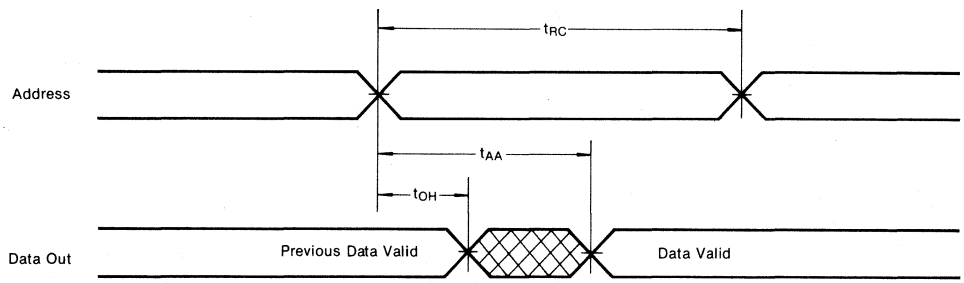
WRITE CYCLE

Parameter	Symbol	KM684000L-5 KM684000L-5L		KM684000L-7 KM684000L-7L		KM684000L-8 KM684000L-8L		KM684000L-10 KM684000L-10L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		100		ns
Chip Select to End of Write	t_{CW}	45		60		70		80		ns
Address Valid to End of Write	t_{AW}	45		60		70		80		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Write Pulse Width	t_{WP}	40		50		55		60		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	25		30		35		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		5		ns

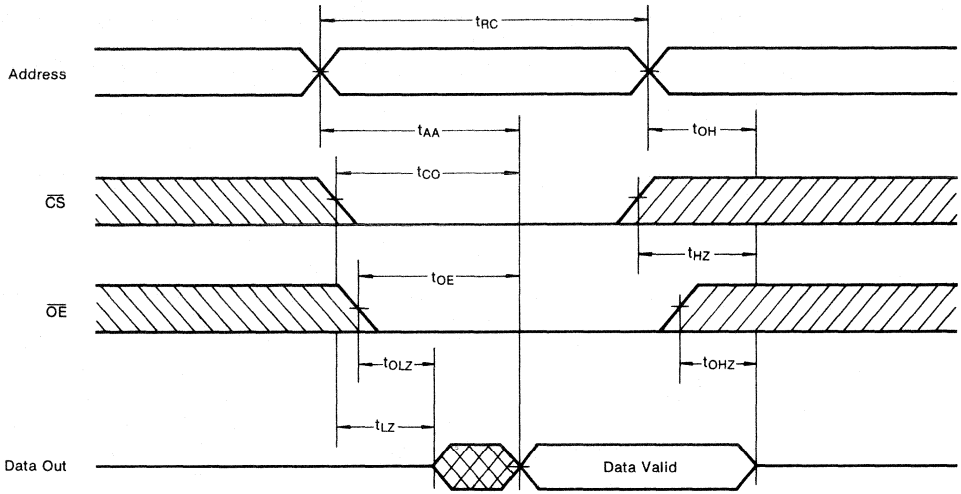
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



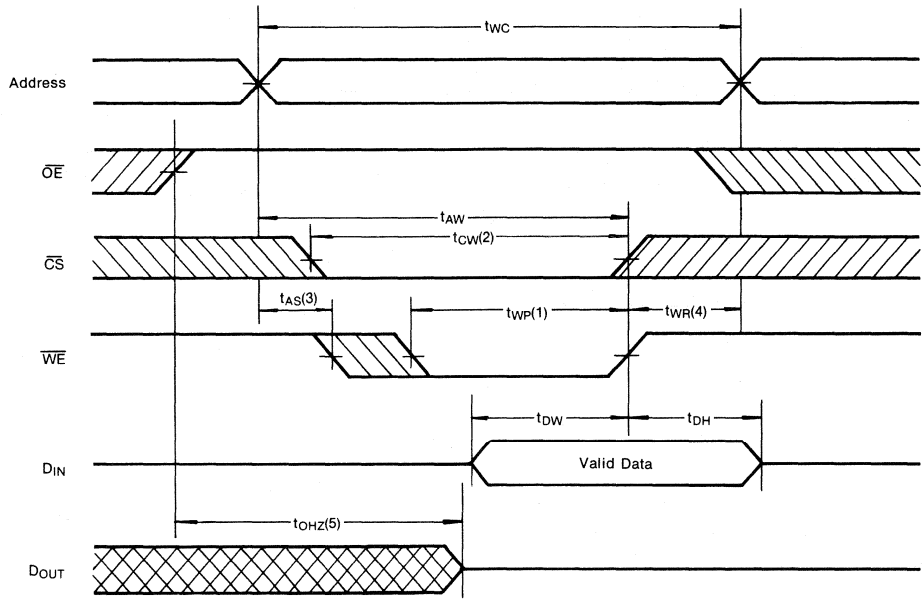
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



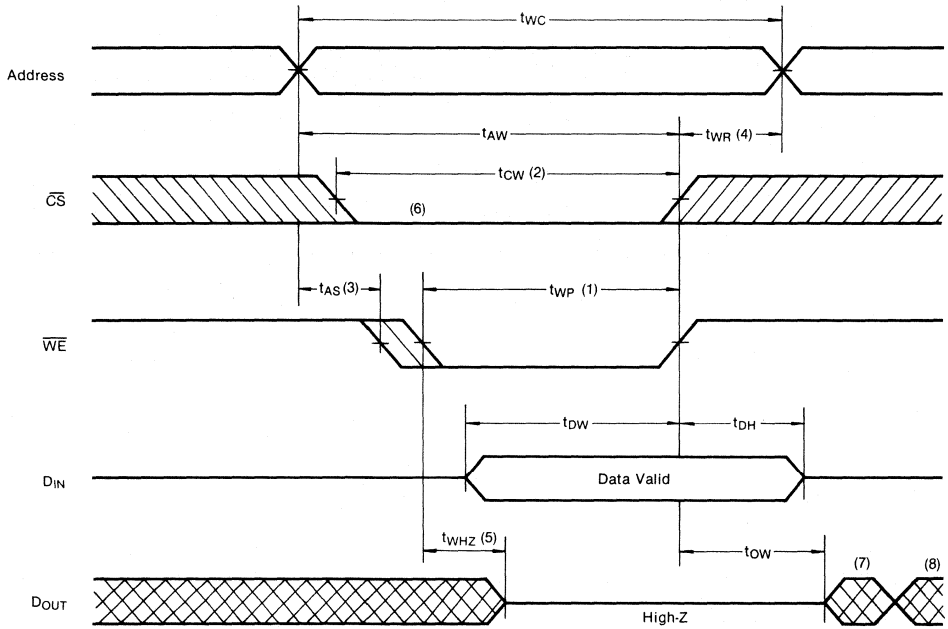
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ = Clock)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ = Low Fixed)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. During this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the some phase of latest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

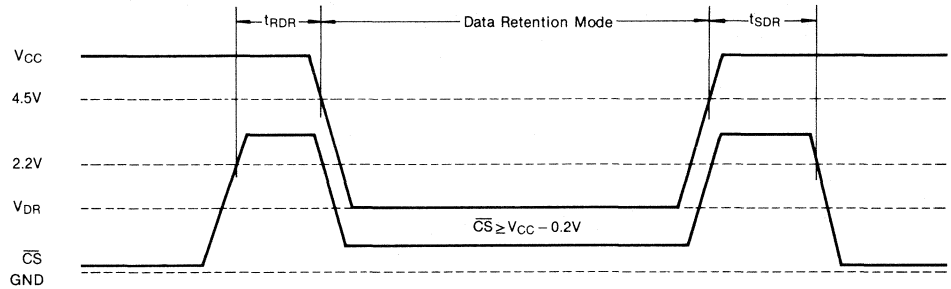
DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3V $\overline{CS} \geq V_{CC} - 0.2V$	L	—	—	50*	μA
			L-L	—	—	10**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)		0			ns
Recovery Time	t_{RDR}			5			ms

* 20μA (Max.) at 0°C~40°C
** 3μA (Max.) at 0°C~40°C

2

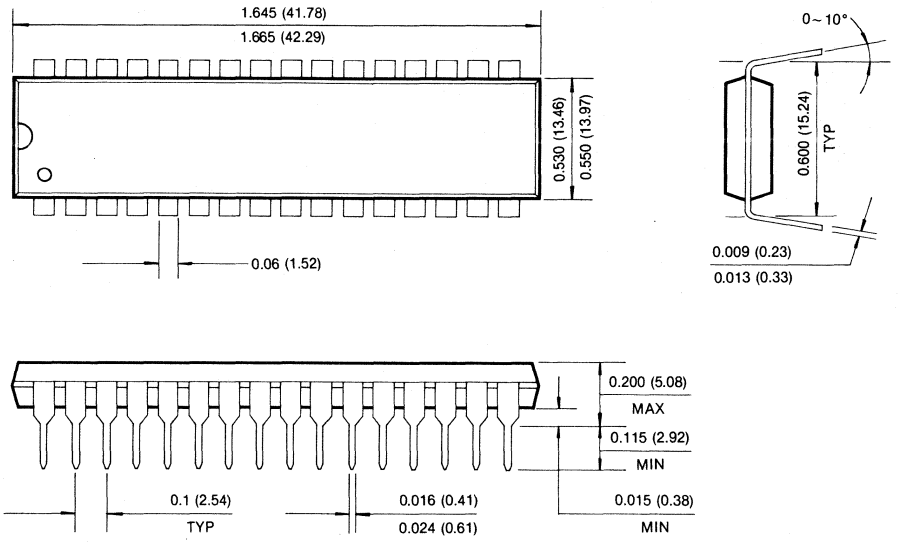
DATA RETENTION WAVEFORM



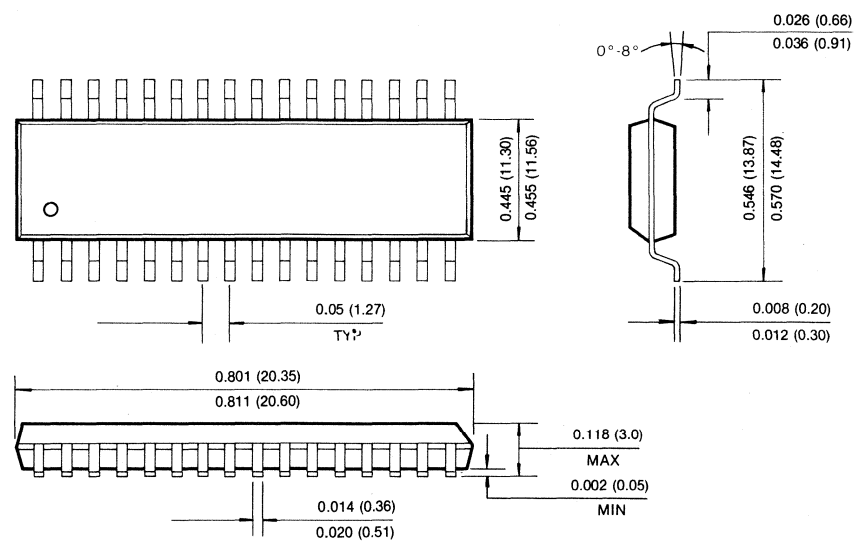
PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (millimeters)

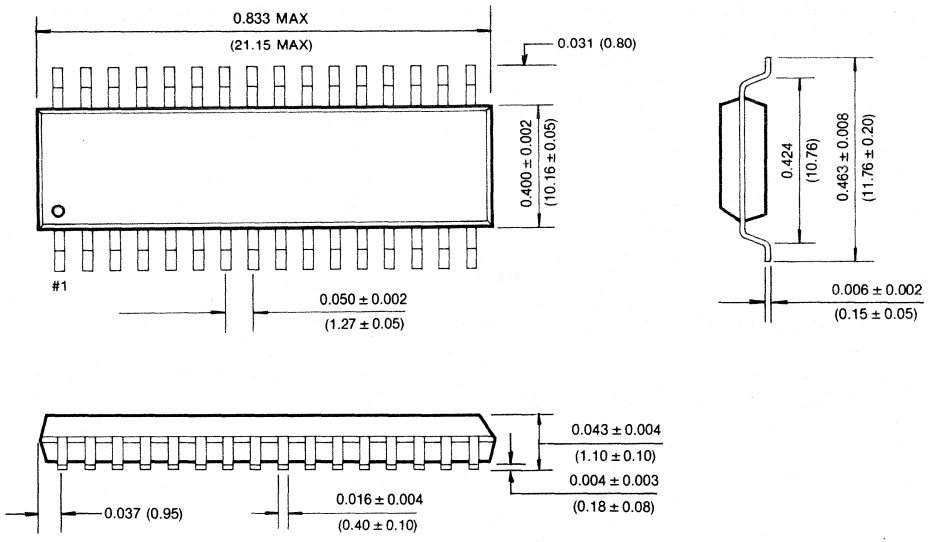


32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil)

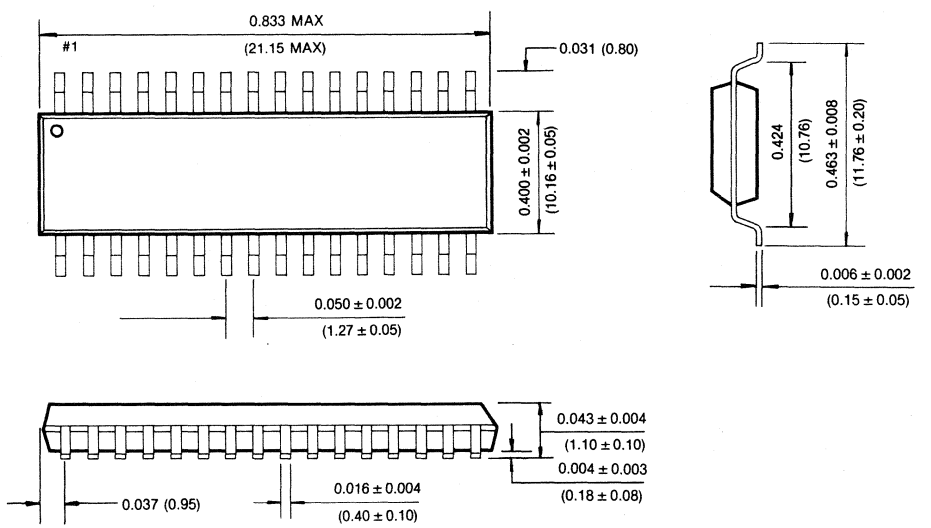


PACKAGE DIMENSIONS

32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (STANDARD TYPE)



32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (REVERSE TYPE)



128K X 8 Bit CMOS Pseudo Static RAM

FEATURES

- **Fast Access Time:**
  - **—$\overline{CE}$ Access Time ... 80,100,120ns (Max.)**
  - **—Cycle Time ... Random Read/Write Cycle Time ... 130,160,190ns (Max.)**
- **Low Power Dissipation ... 200mW typ. (Active) 0.5mW typ. (Standby)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Non multiplexed Address**
- **Three state Output**
- **512 Refresh Cycles/8ms**
- **Self Refresh Current: 1mA (max. Standard) 200μA (max. L-Version) 100μA (max, LL-Version)**
- **Data Retention Supply Voltage; 3.0V to 5.5V**
  - **—Battery Back-up Capability with KM658128LD/LD-L**
- **CS Mode Standby Cycle**
- **32-Pin JEDEC Standard Plastic Package**
  - **—DIP (600mil)**
  - **—SOP (525mil), SOP (450mil)**

GENERAL DESCRIPTION

The KM658128/L/L-L/LD/LD-L is a 1,048,576-bit high-speed Pseudo Static Random Access Memory organized as 131,072 words by 8 bits, fabricated using 1.1μm advanced CMOS technology.

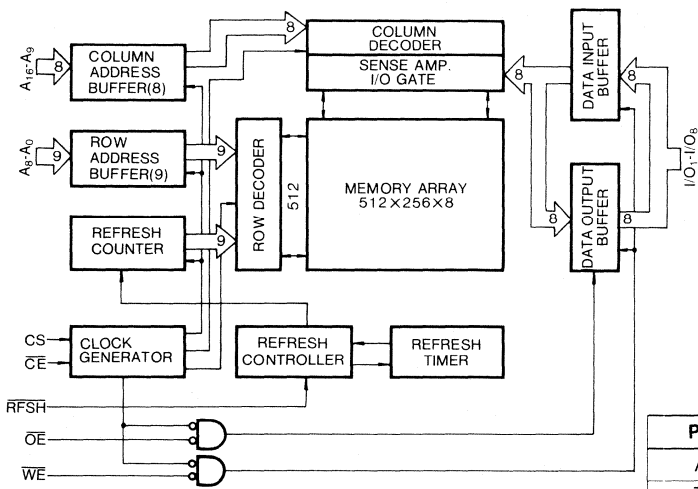
The device, utilizing one transistor DRAM cell with on-chip refresh timer, provides the advantages of DRAM (Low cost, High density) and Static RAM (Low standby power and ease of use).

The pin-out of KM658128/L/L-L/LD/LD-L follow the JEDEC standard for Static RAM with the addition of $\overline{RFSH}$ input. The $\overline{RFSH}$ input allows two types of refresh operation; Auto Refresh and Self Refresh.

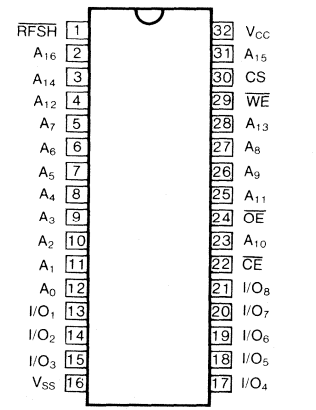
The $\overline{CE}$ only Refresh is also supported.

The KM658128/L/L-L/LD/LD-L supports a write function similiar to static RAM in that the input data is written into the memory cell at the rising edge of $\overline{WE}$, thus simplifying the interface to standard microprocessors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
CS	Chip Select
I/O1-I/O8	Data Inputs/Outputs
VCC	Power Supply
VSS	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Soldering Temperature Time	T_{solder}	260·10 (Lead only)	°C·sec

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating. Section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1.0	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for pulse width≤10ns

DC AND OPERATING CHARACTERISTICS

(Ta=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	All Inputs, V_{IN}=0 to V_{CC}		−10	—	+10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{CC}		−10	—	+10	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}$, CS, Address Cycling I/O=0mA, t_{CYC}=t_{RC}min.	130ns	—	50	70	mA
			160ns	—	40	60	
			190ns	—	35	50	
Standby Power Supply Current	I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{RFSH}$=V_{IH}		—	1	2	mA
	I_{SB2}	$\overline{CE}$≥V_{CC}−0.2V $\overline{RFSH}$≥V_{CC}−0.2V	KM658128	—	—	1	mA
			KM658128L	—	100	200	μA
			KM658128L-L	—	70	100	μA
Self Refresh Current	I_{CC2}	$\overline{CE}$=V_{IH} $\overline{RFSH}$=V_{IL}		—	1	2	mA
	I_{CC3}	$\overline{CE}$≥V_{CC}−0.2V $\overline{RFSH}$≤0.2V	KM658128	—	—	1	mA
			KM658128L	—	100	200	μA
			KM658128L-L	—	70	100	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA		2.4	—	—	V

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	10	pF

* Note: Capacitance is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X*	L	H	OUT	READ
L	H	X	X	L	IN	WRITE
L	H	X	H	H	High-Z	$\overline{CE}$ Refresh
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh
H	X	H	X	X	High-Z	Standby

* Note: X=Don't care

AC CHARACTERISTICS

TEST CONDITIONS (Ta=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified.)

Input Pulse Level ..... 0.6 to 2.6V
Input Rise and Fall Time 5ns
Input Timing Reference Level ..... V_{IH}=2.4V, V_{IL}=0.8V
Output Timing Reference Level ..... V_{OH}=2.2V, V_{OL}=0.8V
Output Load ..... C_L=100pF+1TTL

Item	Symbol	KM658128-8		KM658128-10		KM658128-12		Unit
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	190	—	ns
Random read Modify write Cycle Time	t_{RWC}	190	—	220	—	260	—	ns
Chip Enable Access Time	t_{CEA}	—	80	—	100	—	120	ns
Output Enable Access Time	t_{OEA}	—	30	—	30	—	40	ns
Chip Disable to Output in High-Z	t_{CHZ}	0	30	0	30	0	35	ns
Chip Enable to Output in Low-Z	t_{CLZ}	20		20	—	20	—	ns
Output Disable to Output High-Z	t_{OHZ}	—	25	—	25	—	30	ns
Output Disable Set-Up Time	t_{ODS}	0	—	0	—	0	—	ns
Output Disable Hold Time	t_{ODH}	10	—	10	—	10	—	ns
Output Enable to Output In Low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip Enable Pulse Width	t_{CE}	80n	10μ	100n	10μ	120n	10μ	s
Chip Enable Precharge Time	t_P	40	—	50	—	60	—	ns
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns
Address Hold Time	t_{AH}	30	—	30	—	35	—	ns
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns

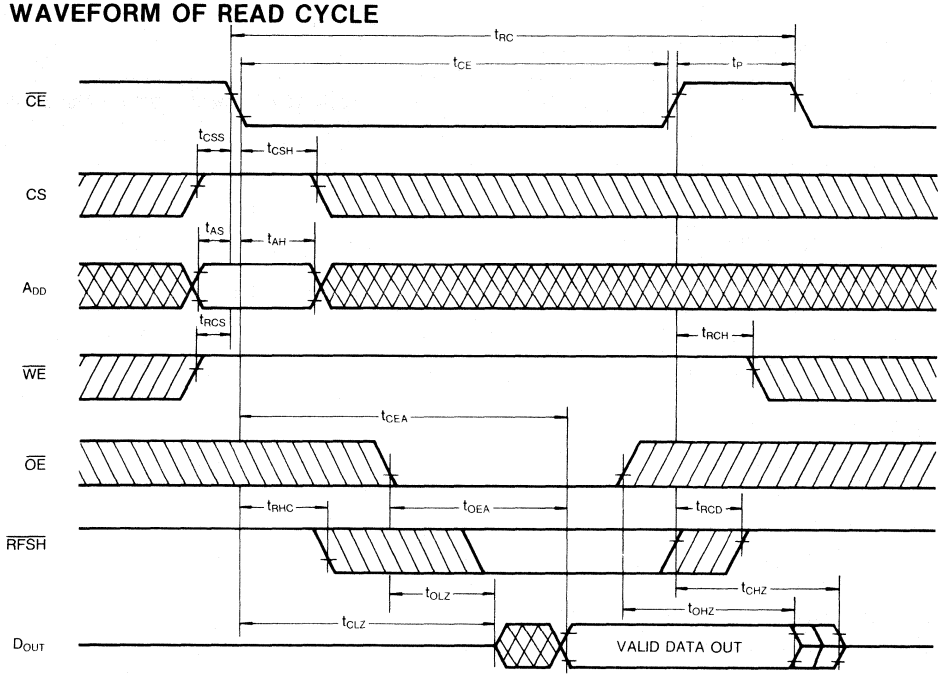
AC CHARACTERISTICS (Continued)

Item	Symbol	KM658128-8		KM658128-10		KM658128-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns
$\overline{RFSH}$ Hold Time	t_{RHC}	15	—	15	—	15	—	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	—	5	—	5	—	5	ns
Chip Select Set-up Time	t_{CSS}	0	—	0	—	0	—	ns
Chip Select Hold Time	t_{CSH}	30	—	30	—	35	—	ns
Write Command Pulse Width	t_{WP}	50	—	60	—	65	—	ns
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns
Data In to End of Write	t_{DW}	25	—	30	—	30	—	ns
Data In Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	ns
Write to Output in High-Z	t_{WHZ}	—	20	—	25	—	30	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	40	—	50	—	60	—	ns
Refresh Precharge Time	t_{FP}	40	—	40	—	40	—	ns
Refresh Reset Time (Automatic Refresh)	t_{RFA}	0	—	0	—	0	—	ns
Refresh Command Pulse Width (Automatic Refresh)	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	190	—	ns
Refresh Command Pulse Width (Self Refresh)	t_{FAS}	8	—	8	—	8	—	μs
Refresh Reset Time (Self Refresh)	t_{RFS}	130	—	160	—	190	—	ns
Refresh Periods (512 cycles)	t_{REF}	—	8	—	8	—	8	ms

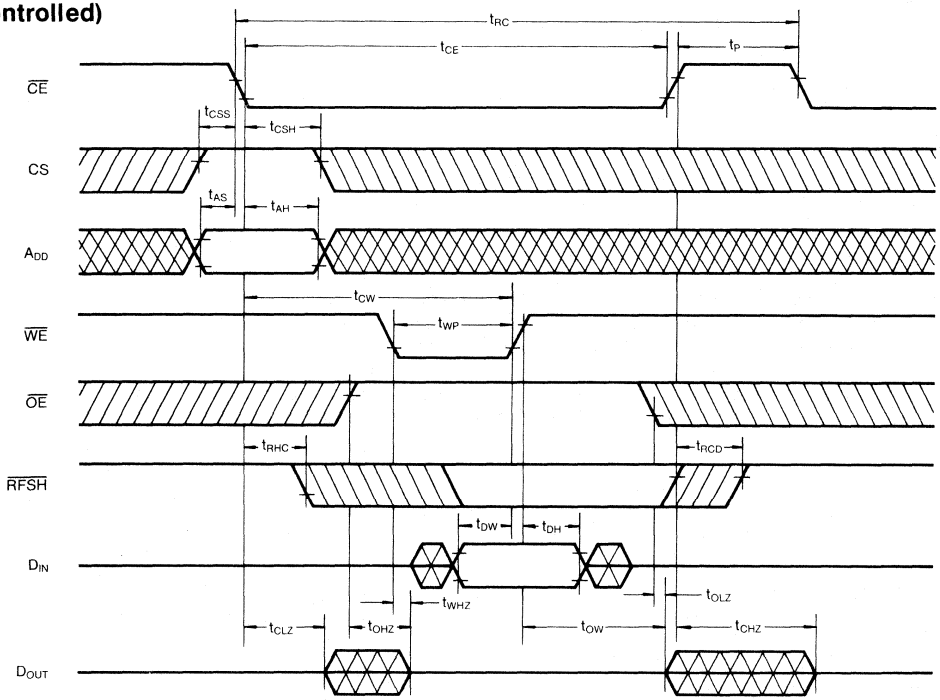
NOTES

1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions under condition of t_T=5ns and are not 100% tested.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under condition of t_T=5ns and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
5. Transition time t_T is measured between V_{IH}(min), and V_{IL}(max).
6. After power-up, pause more than 100μs and execute at least 8 initialization cycle.
7. 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15μs after self refresh, in order to meet the refresh specification of 8ms and 512 cycles.

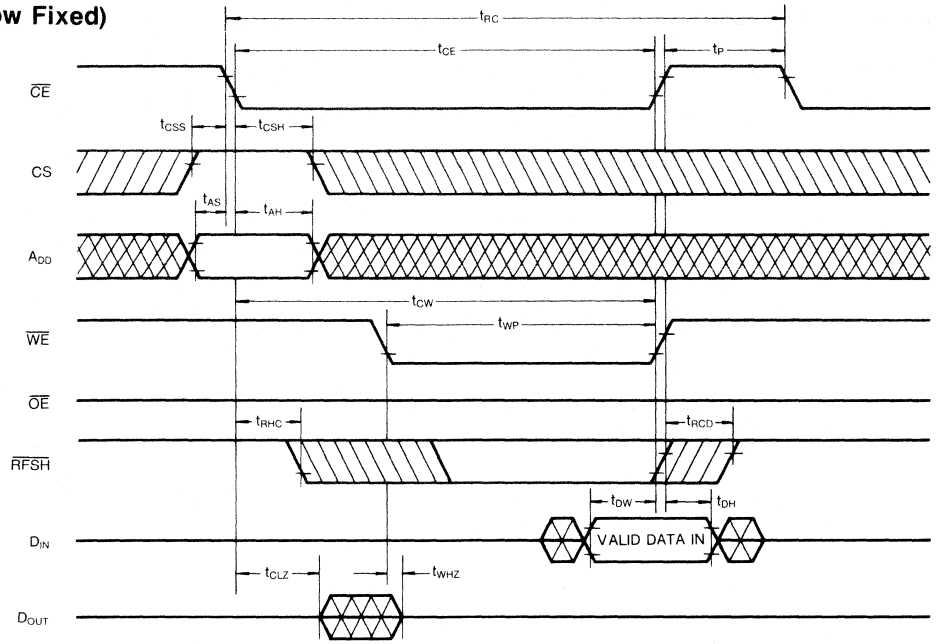
TIMING WAVEFORM OF READ CYCLE



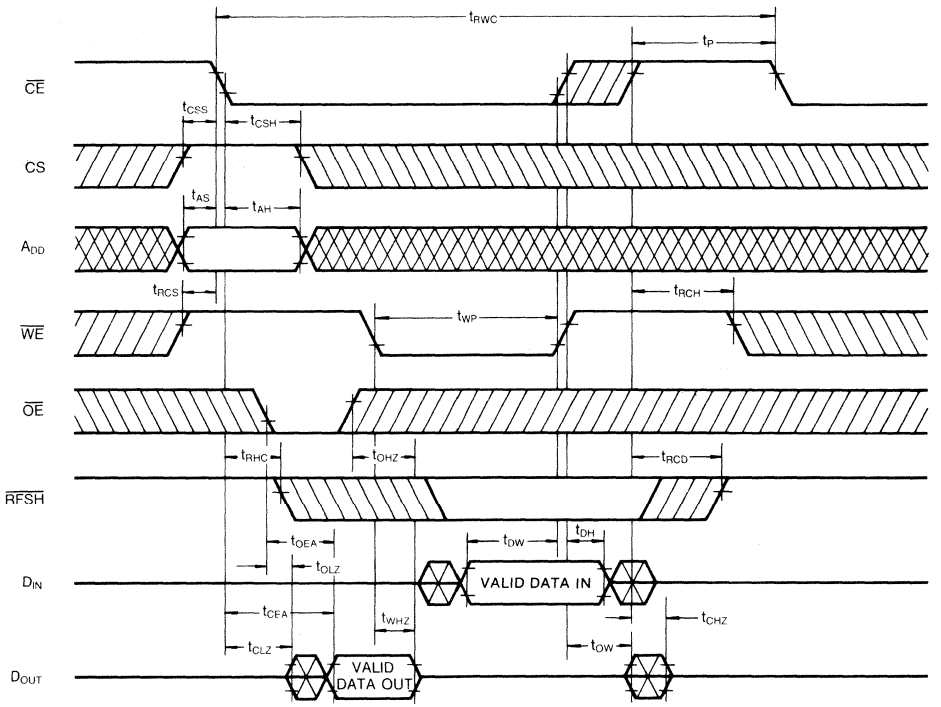
TIMING WAVEFORM OF WRITE CYCLE No. 1 ($\overline{OE}$ Controlled)



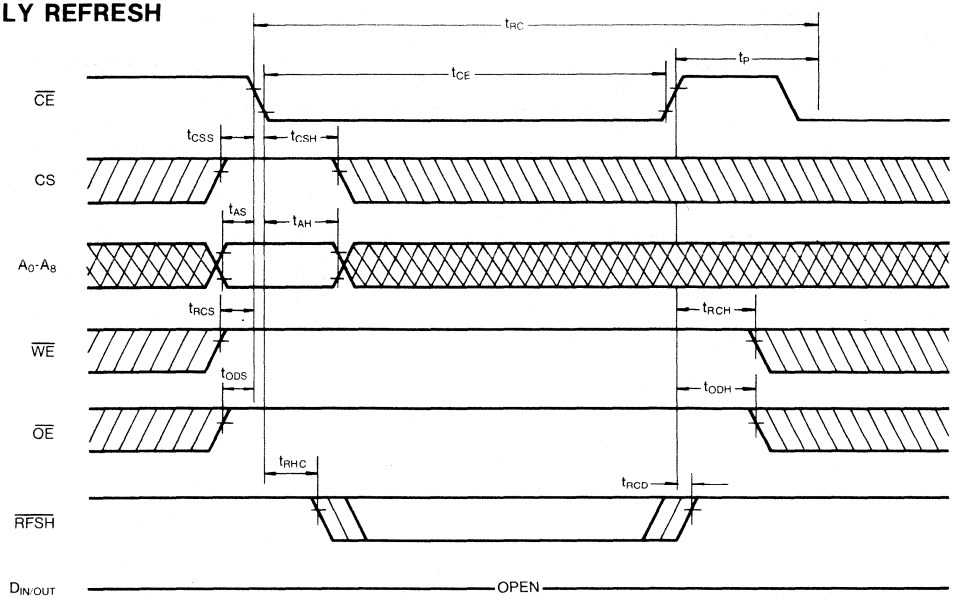
TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{OE}$ Low Fixed)



TIMING WAVEFORM OF READ MODIFY WRITE CYCLE

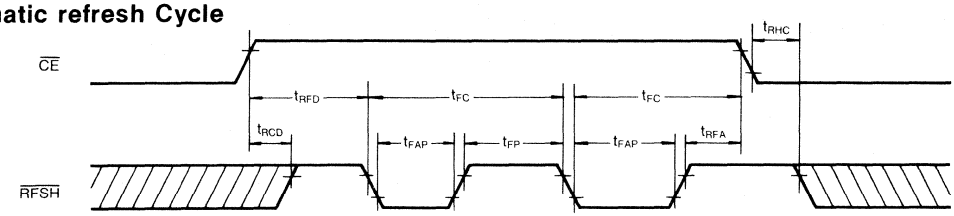


$\overline{CE}$ ONLY REFRESH

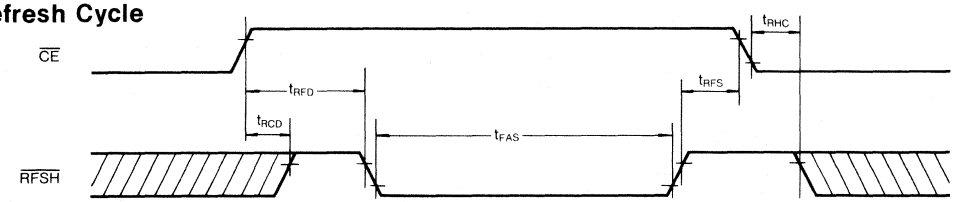


Note: A_{DD9-16} Don't care

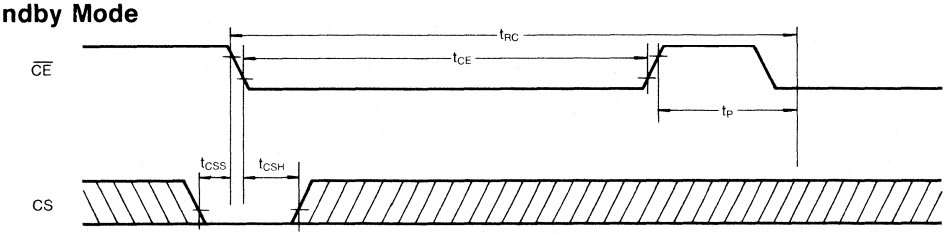
Automatic refresh Cycle



Self refresh Cycle



CS Standby Mode



DATA RETENTION CHARACTERISTICS (Ta=0 to 70°C)

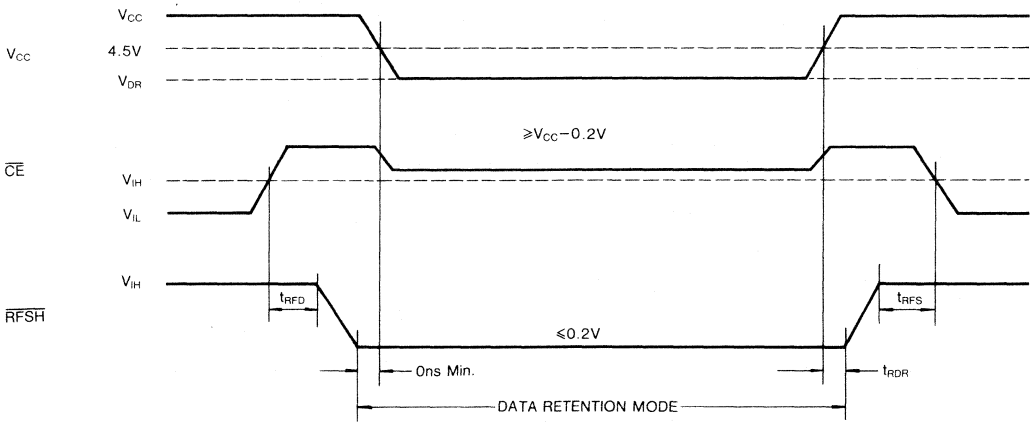
(This characteristics is guaranteed only for LD/LD-L version)

Item		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	3.0	—	5.5	V
Self Refresh Current	V_{DR}=3V	I_{CC3}	—	40	60	μA
(for LD-L Version)	V_{DR}=5.5V		—	70	100	μA
Self Refresh Current	V_{DR}=3V	I_{CC3}	—	40	100	μA
(for LD Version)	V_{DR}=5.5V		—	100	200	μA
Recovery Time		t_{RDR}	5	—	—	ms

Notes: $\overline{CE} \geq V_{CC}-0.2V$ and $\overline{RFSH} \leq 0.2V$

1. The ramping rate of V_{CC} must be greater than |20ms/V| in order to maintain the proper operation of the device, i.e., the transition time from V_{CC} to V_{DR} and V_{DR} to V_{CC} must be greater than 50ms during battery backup data retention mode.
2. Other than data retention mode, self refresh, automatic refresh or $\overline{CE}$ only refresh requires 512 refresh cycles/8ms.
3. During data retention mode, CS, $\overline{OE}$, $\overline{WE}$, A0-A16=Don't Care.

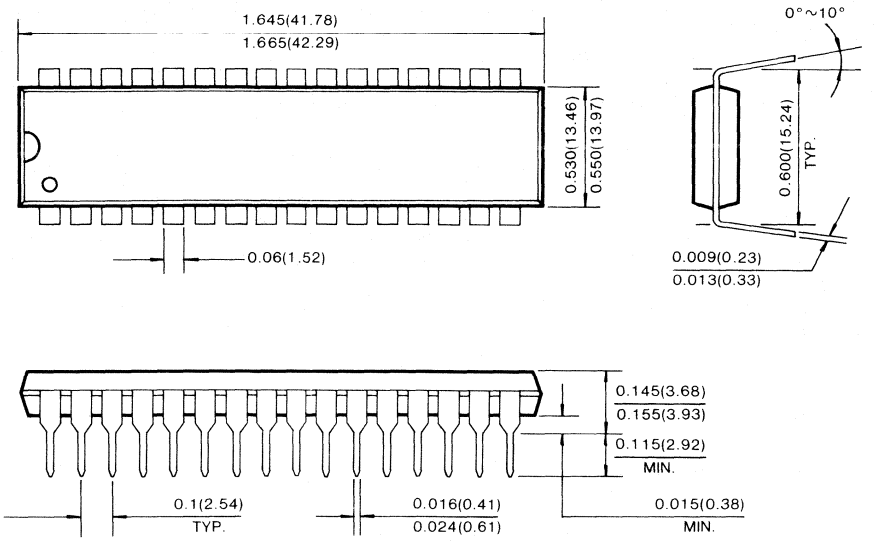
DATA RETENTION WAVEFORM



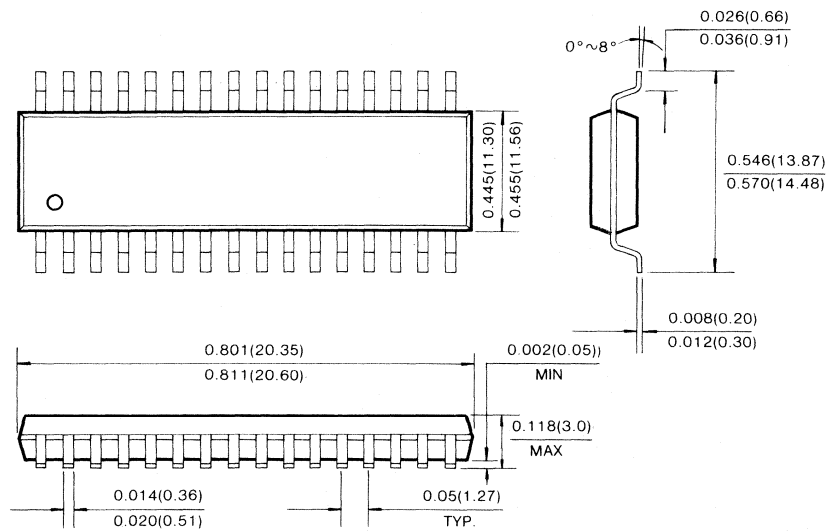
PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil)

Unit: Inches (Millimeters)



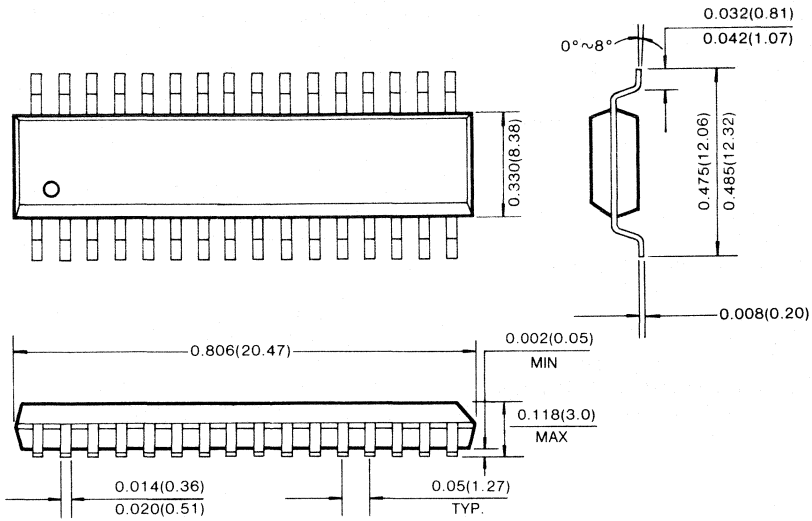
32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil)



PACKAGE DIMENSIONS (Continued)

32 PIN PLASTIC SMALL OUT LINE PACKAGE (450 mil)

Unit: Inches (Millimeters)



524,288 WORD×8 Bit CMOS Pseudo Static RAM

FEATURES

- **Fast Access Time**
  $\overline{CE}$ Access Time: 80, 100, 120ns (Max.)
  Cycle Time: Random Read/Write Cycle Time: 130, 160, 190ns (Max.)
- **Low Power Dissipation: 250mW Typ. (Active)**
  0.5mW Typ. (Standby)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Non Multiplexed Address**
- **Three State Output**
- **2048 Refresh Cycles/32ms**
- **Self Refresh Current: 200μA (Max, L-version)**
  100μA (Max, LL-version)
- **Standard Pin Configuration**
  KM658512P/LP/LP-L: 32-pin DIP (600mil)
  KM658512G/LG/LG-L: 32-pin SOP (525mil)
  KM658512LT/LT-L: 32-pin TSOP (400mil), Standard
  KM658512LR/LR-L: 32-pin TSOP (400mil), Reverse

GENERAL DESCRIPTION

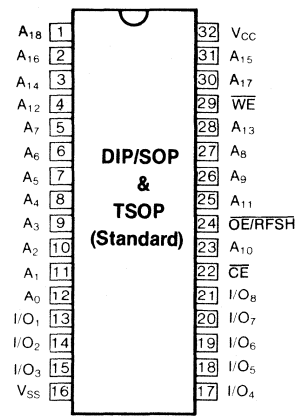
The KM658512L/L-L is a 4,194,304-bits high-speed Pseudo Static Random Access Memory organized as 524,288 words by 8 bits, fabricated using Samsung's advanced CMOS technology.

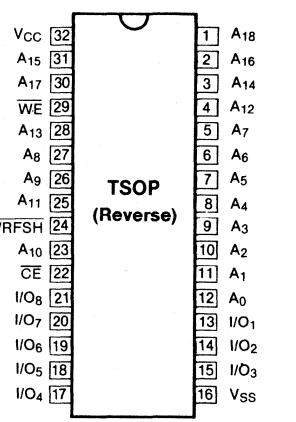
The device, utilizing a one transistor DRAM cell with on-chip refresh timer, provides the advantages of DRAM (Low cost, High density) and Static RAM (Low standby power and ease of use).

The pin-out of KM658512L/L-L follows the JEDEC standard for Static RAM with the addition of $\overline{RFSH}$ input. The $\overline{RFSH}$ input allows two types of refresh operation: Auto Refresh and Self Refresh.

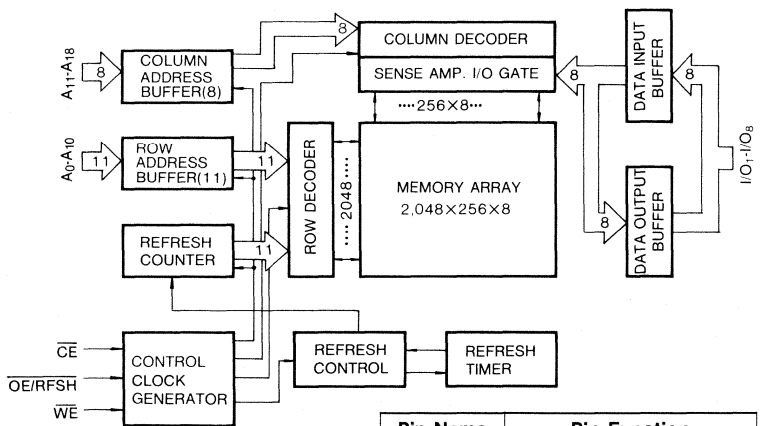
The KM658512L/L-L supports a write function similiar to static RAM in that the input data is written into the memory cell at the rising edge of $\overline{WE}$, thus simplifying the interface to standard microprocessors.

PIN CONFIGURATIONS (Top View)





FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh
$\overline{CE}$	Chip Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to +150	°C
Storage Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Soldering Temperature Time	T_{SOLDER}	260.10	°C.sec

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 1.0	V
Input Low Voltage	V_{IL}	−1.0*	—	0.8	V

* V_{IL}(min.) = −3.0V for pulse width ≤ 10ns

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	All Inputs, V_{IN} = 0 to V_{CC}		−10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}/\overline{RFSH}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}		−10	—	10	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}$, Address Cycling, I/O = 0mA, t_{CYC} = t_{RC} min.	130ns	—	55	75	mA
			160ns	—	45	65	mA
			190ns	—	40	55	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IH}		—	1	2	mA
	I_{SB2}	$\overline{CE}$ ≥ V_{CC} − 0.2V, $\overline{OE}/\overline{RFSH}$ ≥ V_{CC} − 0.2V	KM658512L	—	30	200	μA
			KM658512L-L	—	30	100	μA
Self Refresh Current	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IL}		—	1	2	mA
	I_{CC3}	$\overline{CE}$ ≥ V_{CC} − 0.2V, $\overline{OE}/\overline{RFSH}$ ≤ 0.2V	KM658512L	—	100	200	μA
			KM658512L-L	—	70	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V

FUNCTIONAL DESCRIPTION

$\overline{CE}$	$\overline{OE}$/$\overline{RFSH}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	OUT	READ
L	X	L	IN	WRITE
L	H	H	High-Z	Address Refresh
H	L	X	High-Z	Refresh
H	H	X	High-Z	Standby

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.6 to 2.6V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	$V_{IH} = 2.4V$, $V_{IL} = 0.8V$
Output Timing Reference Level	$V_{OH} = 2.0V$, $V_{OL} = 0.8V$
Output Load	$C_L = 100pF + 1$ TTL

READ CYCLE

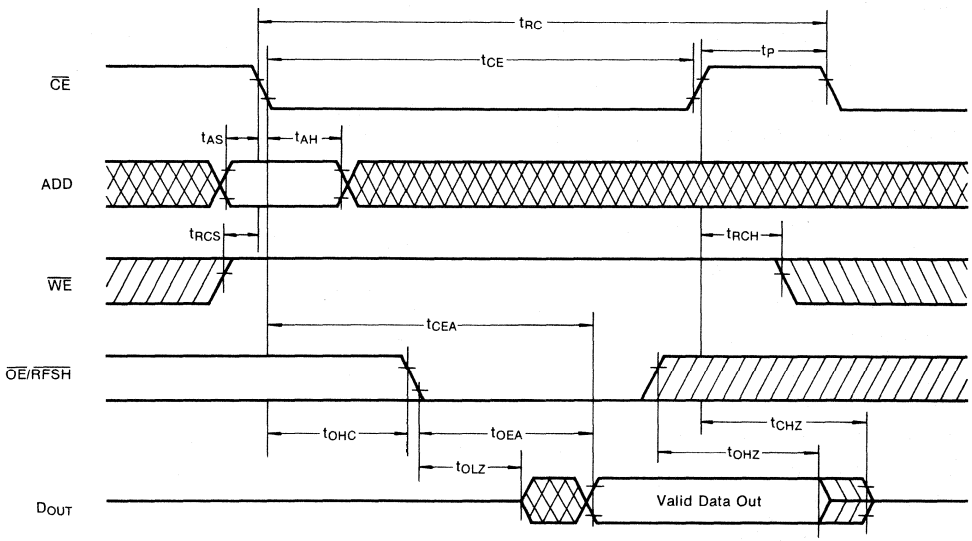
Item	Symbol	KM658512-8		KM658512-10		KM658512-12		Unit
		Min	Max	Min	Max	Min	Max	
Random Read or Write Cycle Time	t_{RC}	130		160		190		ns
Random Read Modify Write Cycle Time	t_{RWC}	180		220		260		ns
Chip Enable Access Time	t_{CEA}		80		100		120	ns
Output Enable Access Time	t_{OEA}		30		40		50	ns
Chip Disable to Output in High-Z	t_{CHZ}	0	25	0	25	0	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}	20		20		20		ns
Output Disable to Output in High-Z	t_{OHZ}		25		25		30	ns
Output Enable to Output in Low-Z	t_{OLZ}	0		0		0		ns
Chip Enable to Output Enable Dlay Time	t_{OCD}	0		0		0		ns
Output Enable Hold Time	t_{OHC}	15		15		15		ns
Chip Enable Pulse Width	t_{CE}	80	10	100	10	120	10	μs
Chip Enable Precharge Time	t_P	40		50		60		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	20		25		30		ns
Read Command Set-up Time	t_{RCS}	0		0		0		ns
Read Command Hold Time	t_{RCH}	0		0		0		ns
Write Command Pulse Width ($\overline{OE}$ = high)	t_{WP}	25		30		35		ns
Write Command Pulse Width ($\overline{OE}$ = Low)	t_{WP}	45		55		65		ns
Chip Enable to End of Write	t_{CW}	80		100		120		ns
Data In to End of Write	t_{DW}	20		25		30		ns
Data In Hold Time for Write	t_{DH}	0		0		0		ns
Output Active from End of Write	t_{OW}	5		5		5		ns
Write to Output in High-Z	t_{WHZ}		20		25		30	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	40		50		60		ns
Refresh Precharge Time	t_{FP}	40		40		40		ns
Refresh Command Pulse Width (Automatic Refresh)	t_{FAP}	80	8000	80	8000	80	8000	ns
Automatic Refresh Cycle Time	t_{FC}	130		160		190		ns
Refresh Command Pulse Width (Self Refresh)	t_{FAS}	8		8		8		μs
Refresh Reset Time (Self Refresh)	t_{RFS}	130		160		190		ns
Refresh Periods (2048 cycles)	t_{REF}		32		32		32	ms

Notes:

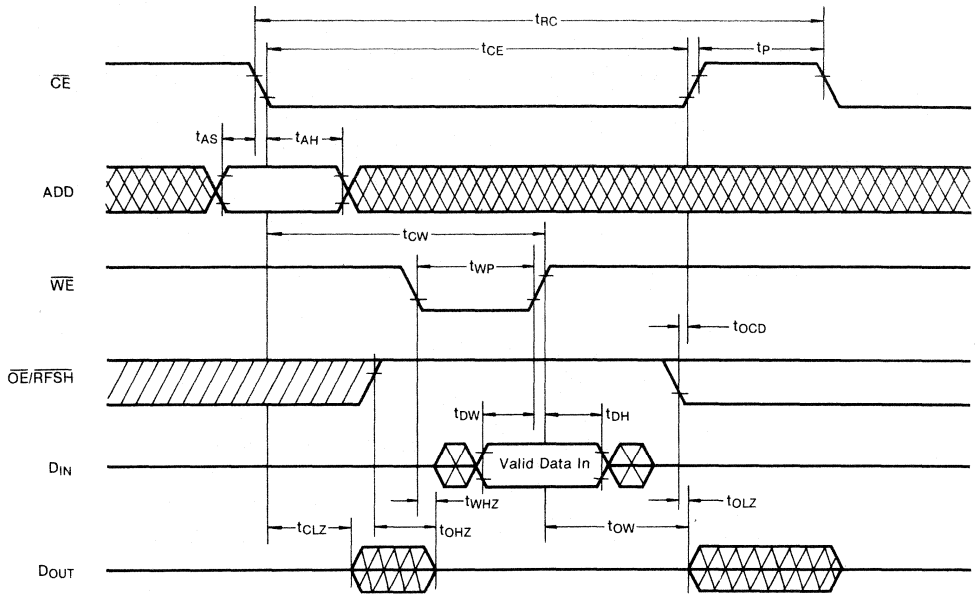
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of $t_T = 5ns$ and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
5. Transition time t_T is measured between V_{IH} (min.) and V_{IL} (max.).
6. After power-up, pause for more than 100μs and execute at least 8 initialization cycles.
7. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15μs after self refresh, in order to meet the refresh specification of 32ms and 2048 cycles.

TIMING DIAGRAMS

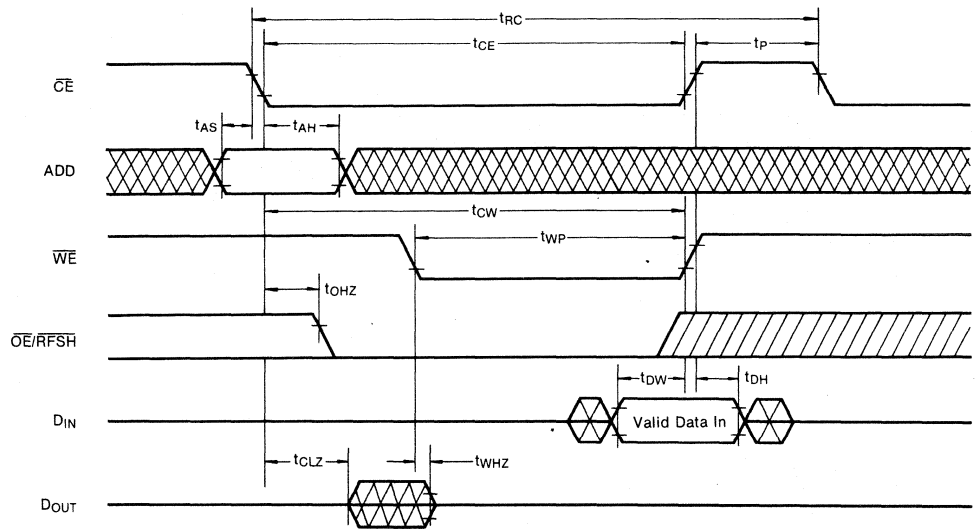
TIMING WAVEFORM OF READ CYCLE



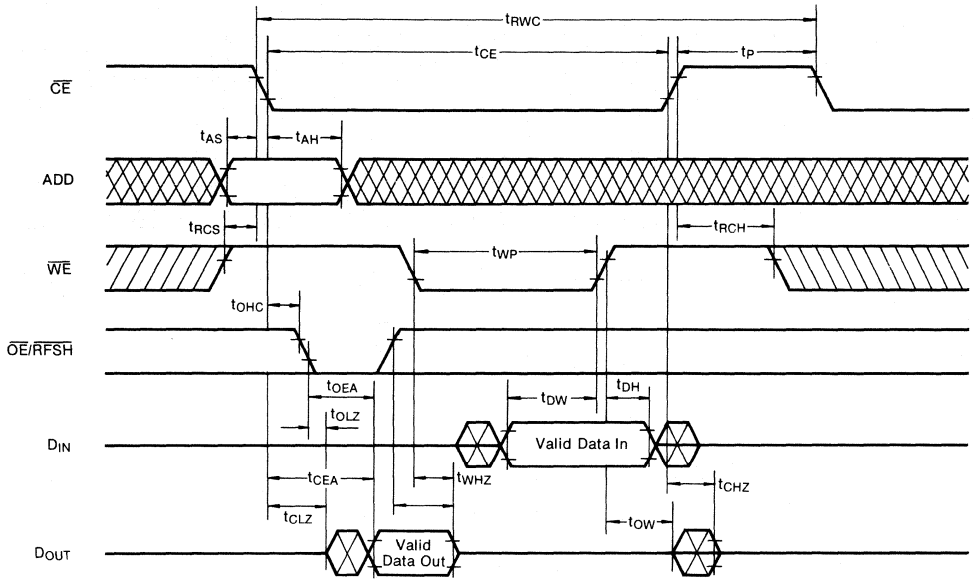
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ High)



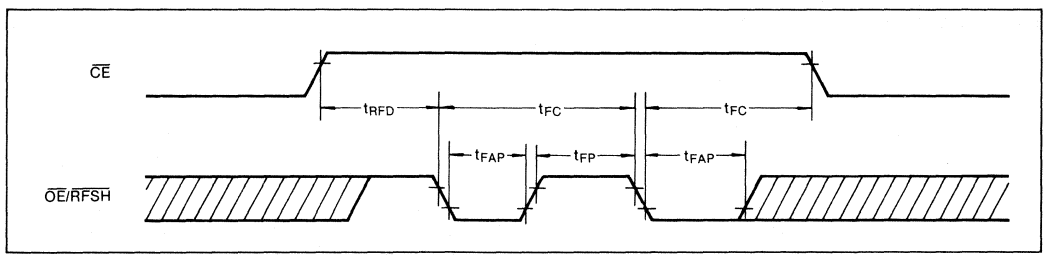
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{OE}$ Low)



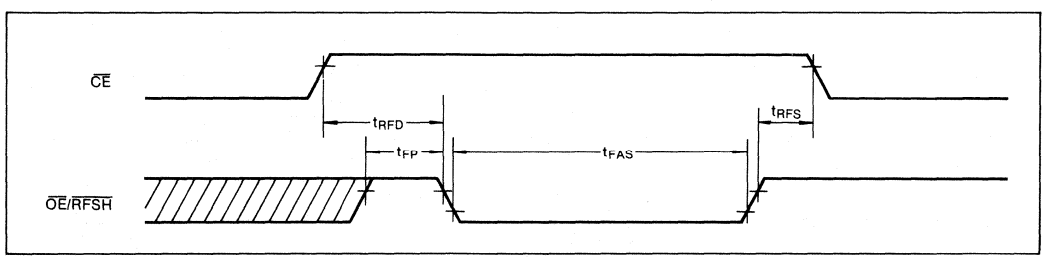
TIMING WAVEFORM OF READ MODIFY WRITE CYCLE



Automatic Refresh Cycle

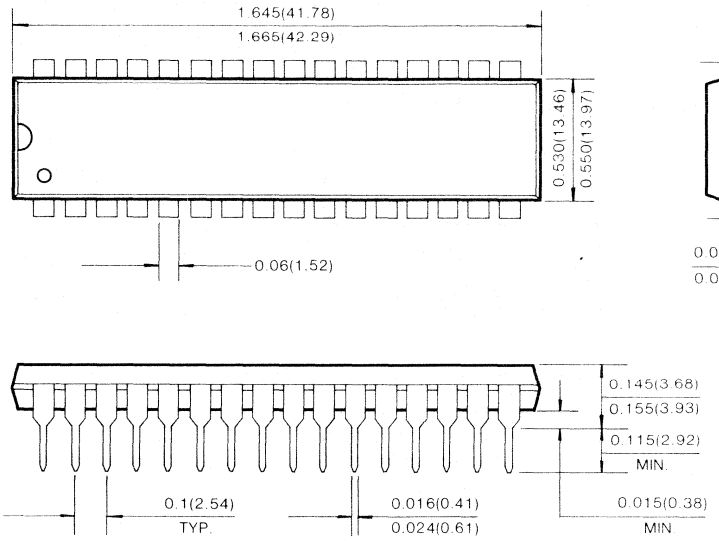


Self Refresh Cycle

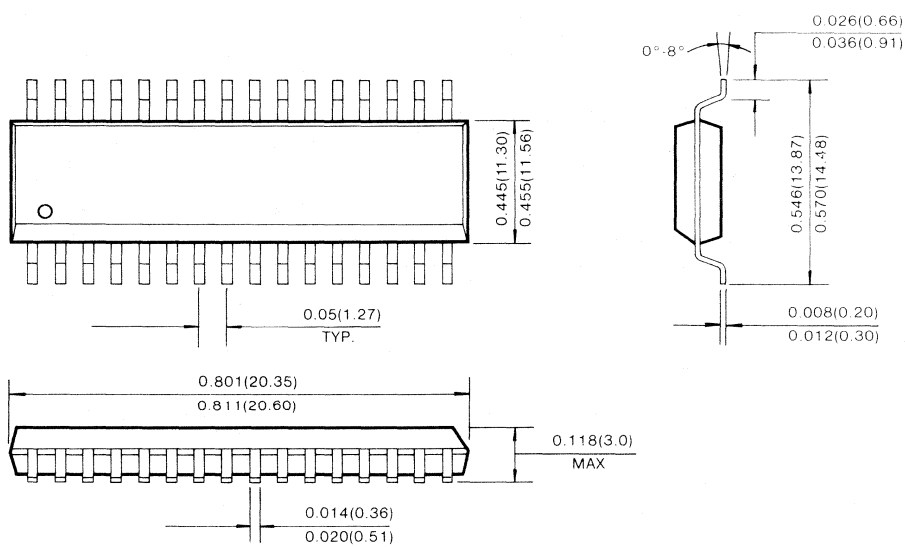


PACKAGE DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (600 mil.)

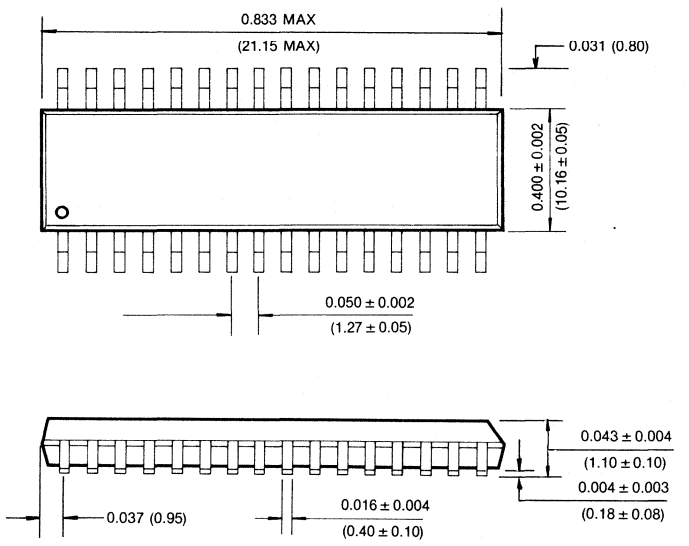


32 PIN PLASTIC SMALL OUT LINE PACKAGE (525 mil.)

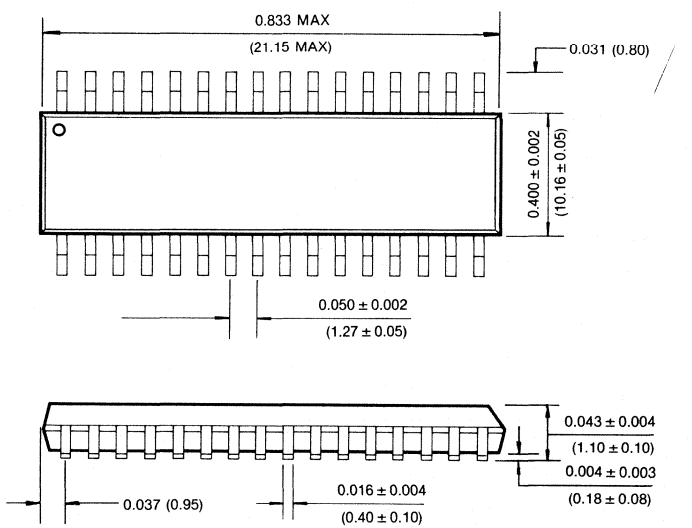


PACKAGE DIMENSIONS

32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (STANDARD TYPE)



32 PIN PLASTIC THIN SMALL OUT LINE PACKAGE (REVERSE TYPE)



16K×4 Bit Static RAM

FEATURES

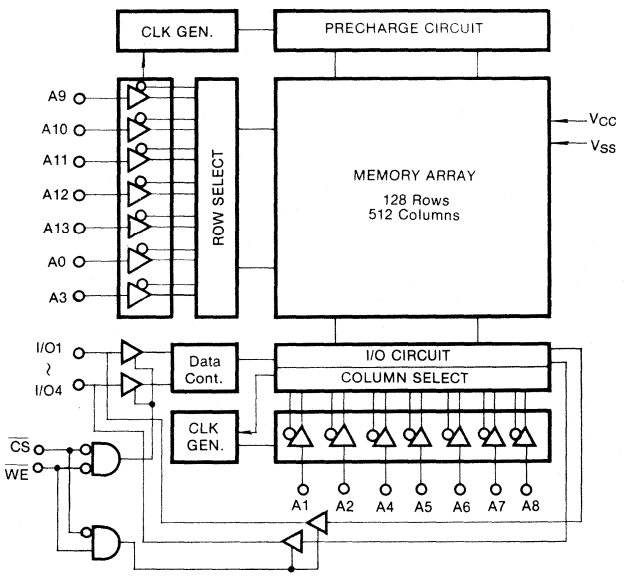
- **Fast Access Time: 25, 35, 45ns (max.)**
- Low Power Dissipation
  - Standby (TTL) : **30mA (max.)**
  - (CMOS): 2mA (max.)
  - 100μA (max.) L-Version
  - Operating : 120mA (max.)
- Single 5V±10% Power Supply
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Current: 50 μA (max.)**
- **Battery Back-up Operation**
  - **2V (min.) Data Retention**
- **Standard Pin Configuration**
  KM6465AP/ALP: 22-pin DIP (300 mil.)

GENERAL DESCRIPTION

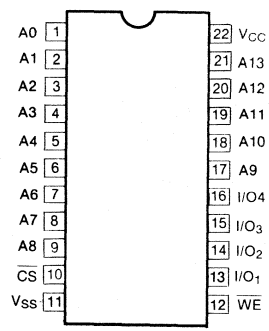
The KM6465A/AL is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM6465A/AL has a chip select input for the minimum current power down mode.
The KM6465A/AL has been designed for high speed applications. It is particularly well suited for the use in high speed and low power nonvolatility is required.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



(DIP)

Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	0 to 70	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*		0.8	V

* V_{IL}(min) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified.)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{OUT} = V_{SS}$ to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			2	mA
			L		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	6	pF

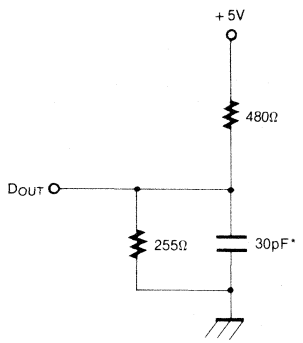
*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

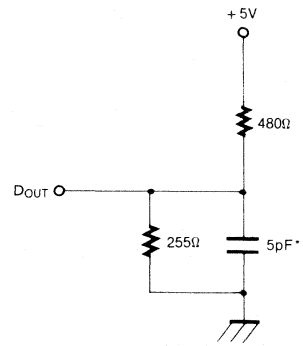
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6465A-25 KM6465AL-25		KM6465A-35 KM6465AL-35		KM6465A-45 KM6465AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{CO}		25		35		45	ns
Chip Select to Low-Z Output	t_{LZ}	5		7		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		20		30		30	ns

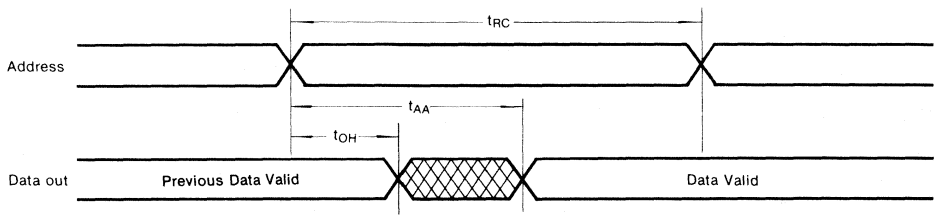
WRITE CYCLE

Parameter	Symbol	KM6465A-25 KM6465AL-25		KM6465A-35 KM6465AL-35		KM6465A-45 KM6465AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		40		ns
Chip Select to End of Write	t_{CW}	25		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	25		30		40		ns
Write Pulse Width	t_{WP}	25		25		30		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	10	0	15	0	15	ns
Data to Write Time Overlap	t_{DW}	15		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

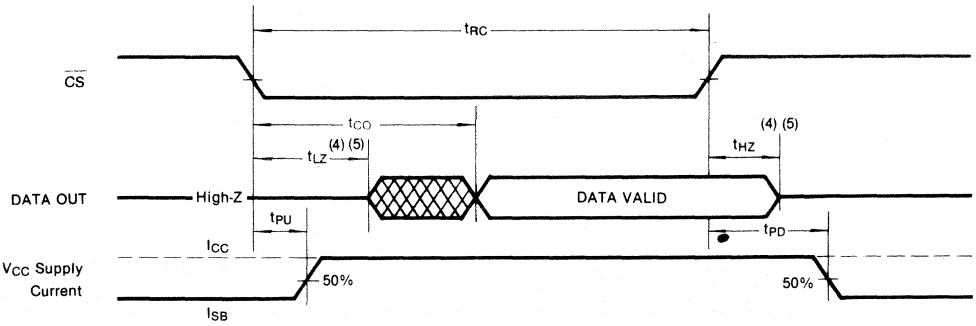
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}=V_{IL}$, $\overline{WE}=V_{IH}$)



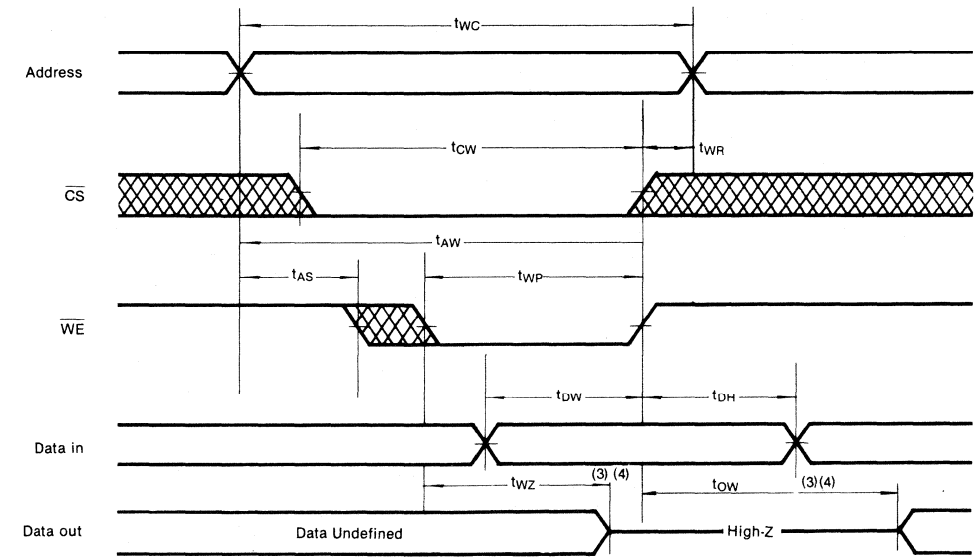
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



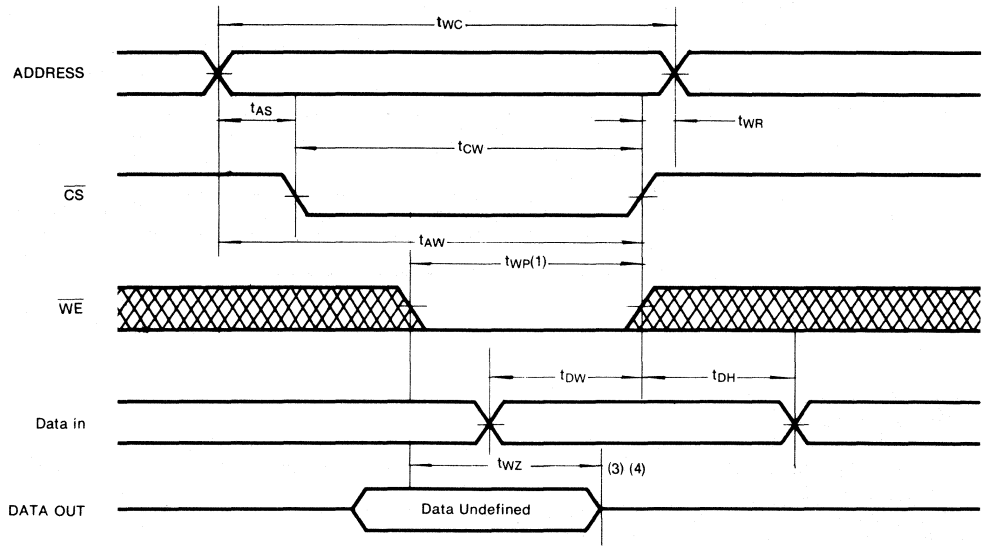
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	I/O PIN	Supply Current	Mode
H	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC}	Read
L	L	D_{IN}	I_{CC}	Write

*Note: X means Don't Care

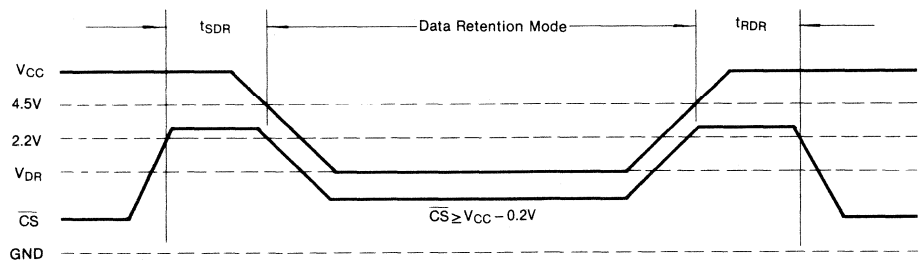
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(Guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1.0	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

*t_{RC} = Read Cycle Time

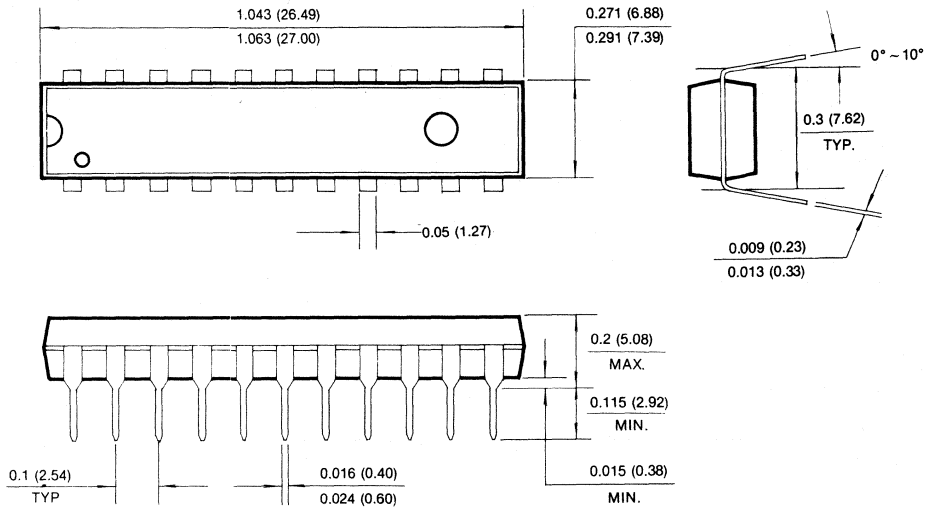
DATA RETENTION WAVEFORM



PACKAGE DIMENSIONS

22 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



16,384 WORD×4 Bit CMOS Static RAM

FEATURES

- **Fast Access Time: 12, 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 35mA (max.)
  (CMOS): 1mA (max.)
  100μA (max.) L-Version
- **Operating KM6465BP/J-12: 140mA (max.)**
  KM6465BP/J-15: 130mA (max.)
  KM6465BP/J-20: 120mA (max.)
  KM6465BP/J-25: 110mA (max.)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  No clock or refresh required
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (min.)**
- **Standard 22-pin DIP (300 mil.)**

GENERAL DESCRIPTION

The KM6465B/BL is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bits.

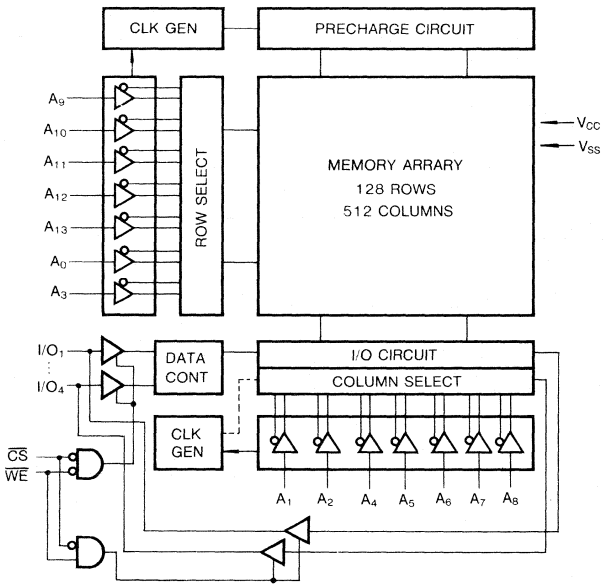
The device is fabricated using Samsung's advanced CMOS process.

The KM6465B/BL has a chip select input for the minimum current power down mode.

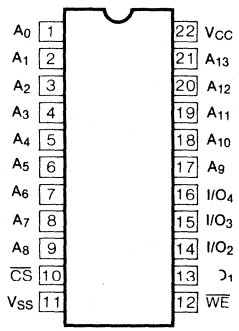
The KM6465B/BL has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}, V_{CC} = Max		—	—	1	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	12ns	—	110	140	mA
			15ns	—	95	130	mA
			20ns	—	85	120	mA
			25ns	—	75	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$		—	15	35	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$		—	—	1	mA
		$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L		2	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note: Capacitance is sampled and not 100% tested.

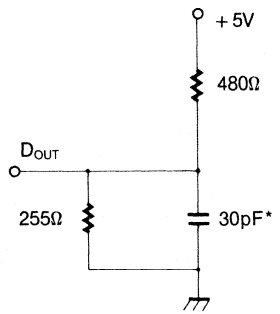
AC CHARACTERISTICS

TEST CONDITIONS

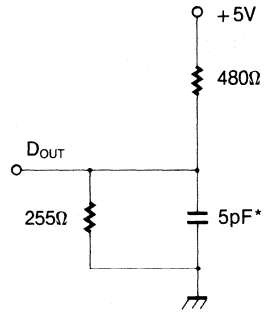
($T_A = 0$ to 70°C, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Loads	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{OW}, t_{LZ} & t_{WZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6465BP-12 KM6465BJ-12		KM6465BP-15 KM6465BJ-15		KM6465BP-20 KM6465BJ-20		KM6465BP-25 KM6465BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AA}		12		15		20		25	ns
Chip Select to Output	t_{CO}		12		15		20		25	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		12		15		20		25	ns

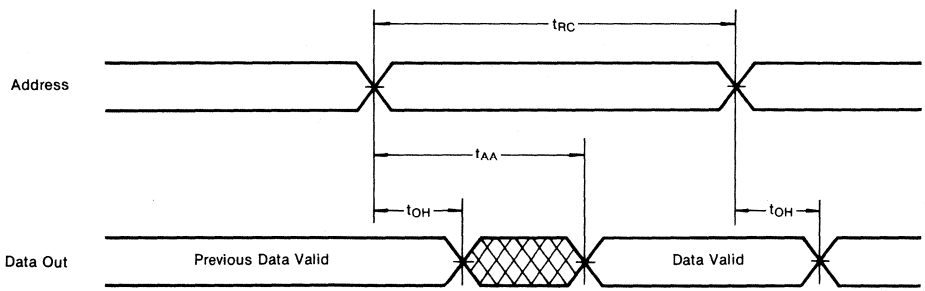
WRITE CYCLE

Parameter	Symbol	KM6465BP-12 KM6465BJ-12		KM6465BP-15 KM6465BJ-15		KM6465BP-20 KM6465BJ-20		KM6465BP-25 KM6465BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	10		12		13		15		ns
Write Pulse Width	t_{WP}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

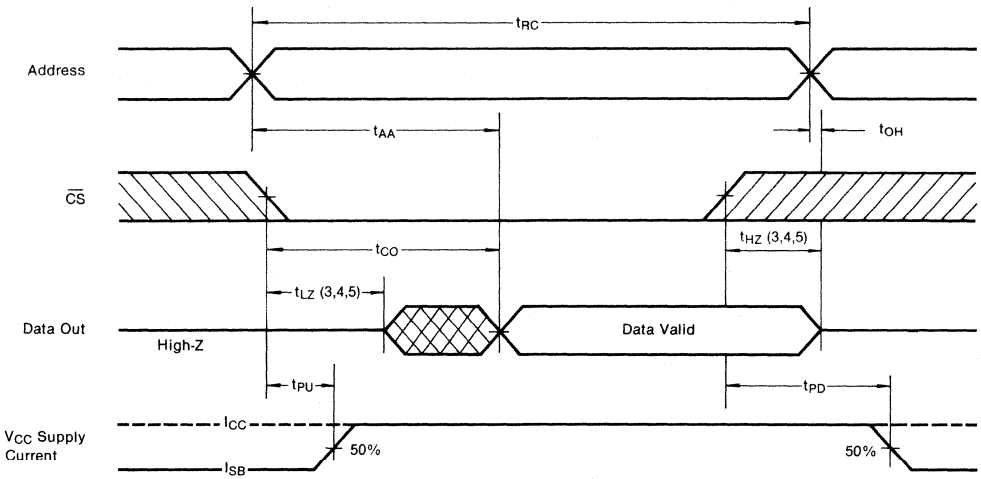
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH})



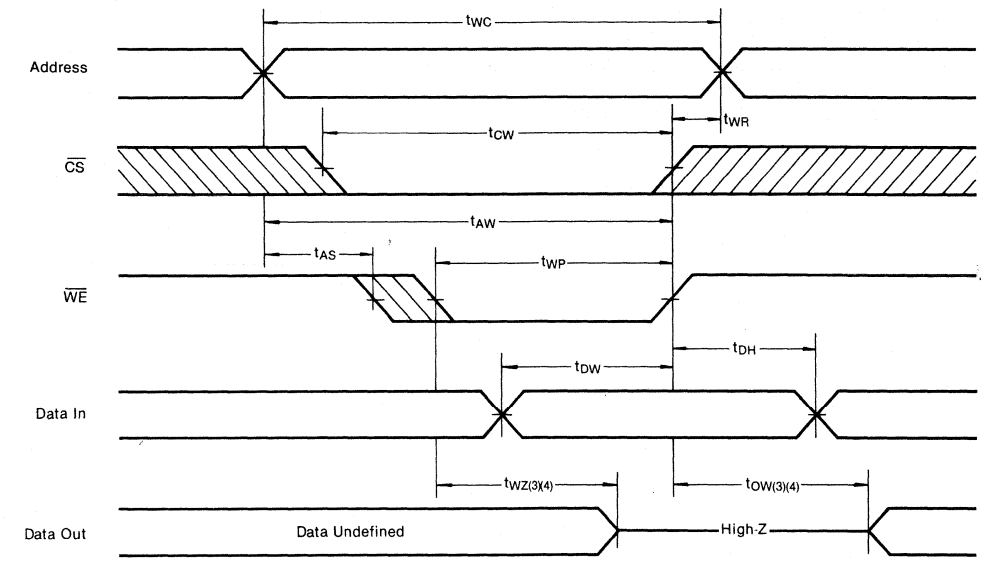
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



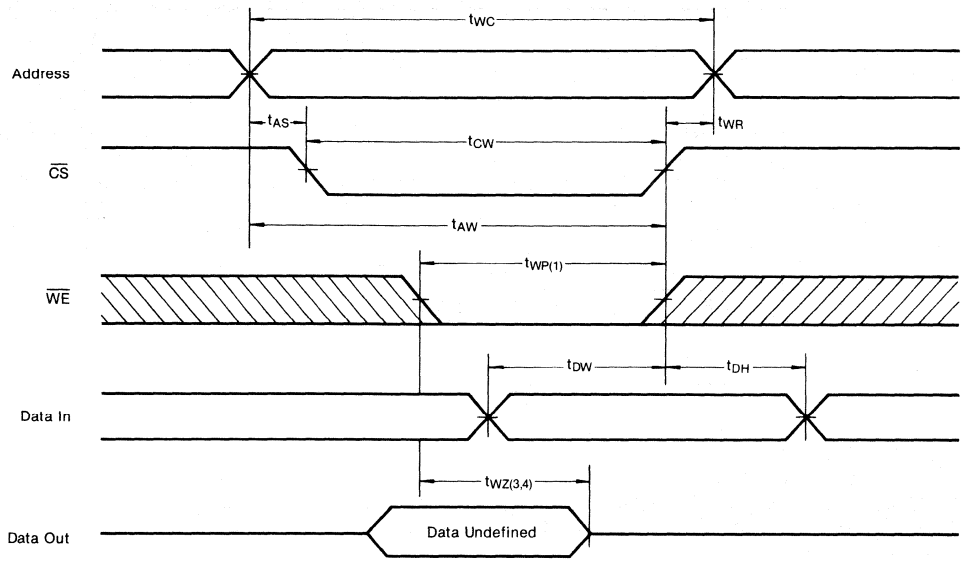
Notes (Read Cycle):

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ} (min) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	I/O Pin	Supply Current	Mode
H	X*	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC}	Read
L	L	D_{IN}	I_{CC}	Write

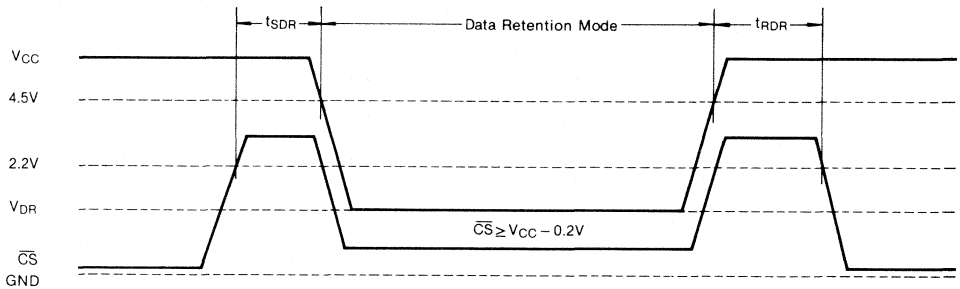
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2		5.5	V
Data Retention Current	I_{DR}	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	50*	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}**			ns

*: V_{CC} = 3V
**: t_{RC} = Read Cycle Time

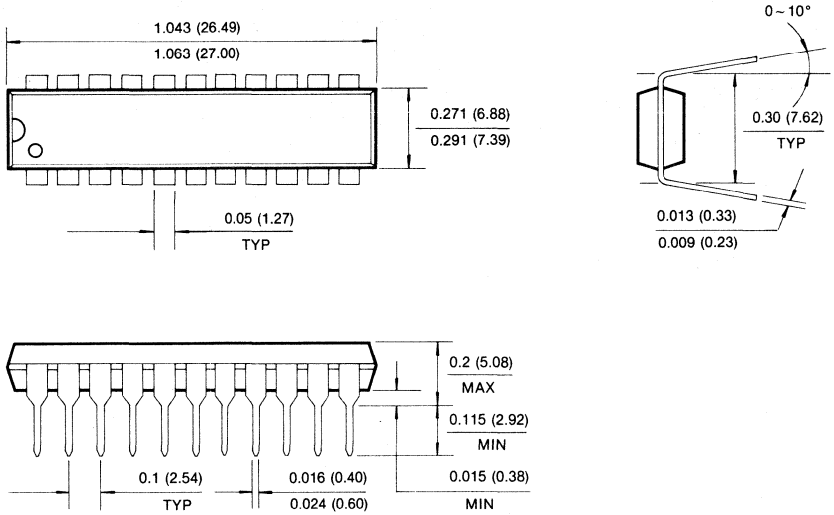
DATA RETENTION WAVEFORM



PACKAGE DIMENSION

22 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



16K×4 Bit Static RAM (with $\overline{OE}$)

FEATURES

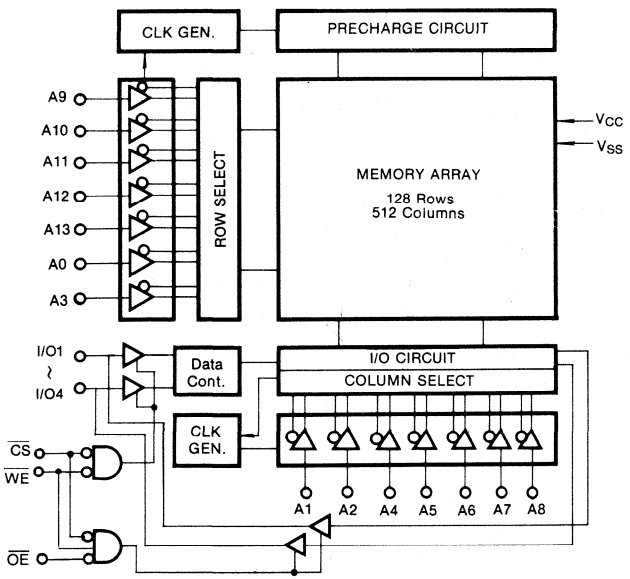
- **Fast Access Time: 25,35,45 ns (max.)**
- **Low Power Dissipation**
  Standby (TTL): 30mA (max.)
  (CMOS): 2mA (max.)
  100μA (max.) L-Version
  Operating: 120mA (max.)
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  —No clock or refresh required
- **Three State Outputs**
- **Low Data Retention Current: 50μA (min.)**
- **Battery Back-up Operation**
  —2V (min.) Data Retention
- **Standard Pin Configuration**
  KM6466AP/ALP: 24-pin DIP (300 mil.)
  KM6466AJ/ALJ: 24-pin SOJ (300 mil.)

GENERAL DESCRIPTION

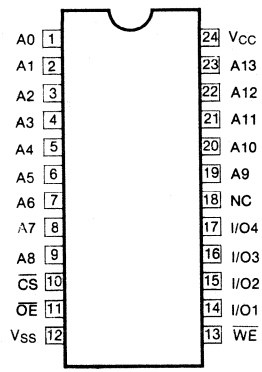
The KM6466A/AL is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bit.
The device is fabricated using Samsung's advanced CMOS process.
The KM6466A/AL has a chip select input for the minimum current power down mode.
The KM6466A/AL has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	0 to 70	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$			2	mA
			L		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	6	pF

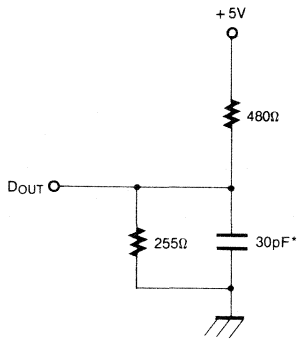
*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

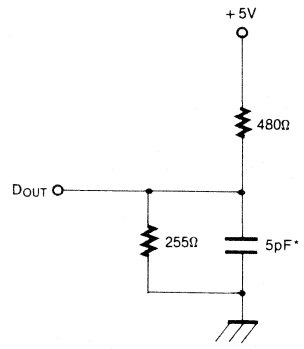
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6466A-25 KM6466AL-25		KM6466A-35 KM6466AL-35		KM6466A-45 KM6466AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{CO}		25		35		45	ns
Output Enable to Output	t_{OE}		15		15		20	ns
Output Enable to Low-Z Output	t_{OLZ}	5		7		7		ns
Output Disable to to High-Z Output	t_{OHZ}	0	15	0	15	0	15	ns
Chip Enable to Low-Z Output	t_{LZ}	5		7		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		20		30		30	ns

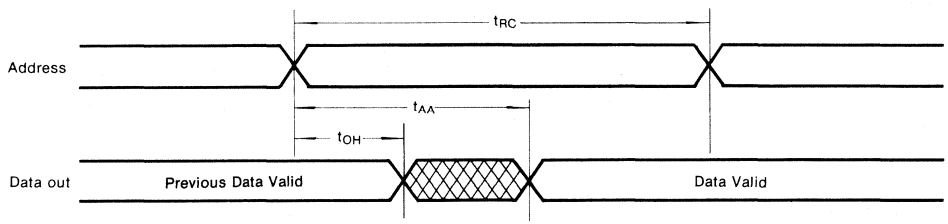
WRITE CYCLE

Parameter	Symbol	KM6466A-25 KM6466AL-25		KM6466A-35 KM6466AL-35		KM6466A-45 KM6466AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		40		ns
Chip Select to End of Write	t_{CW}	25		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	25		30		40		ns
Write Pulse Width	t_{WP}	25		25		30		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	10	0	15	0	15	ns
Data to Write Time Overlap	t_{DW}	15		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

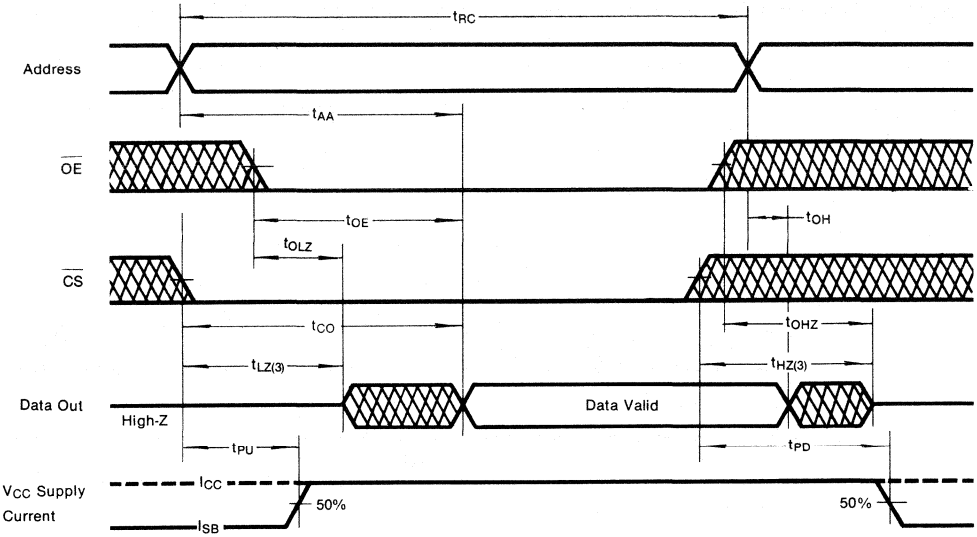
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



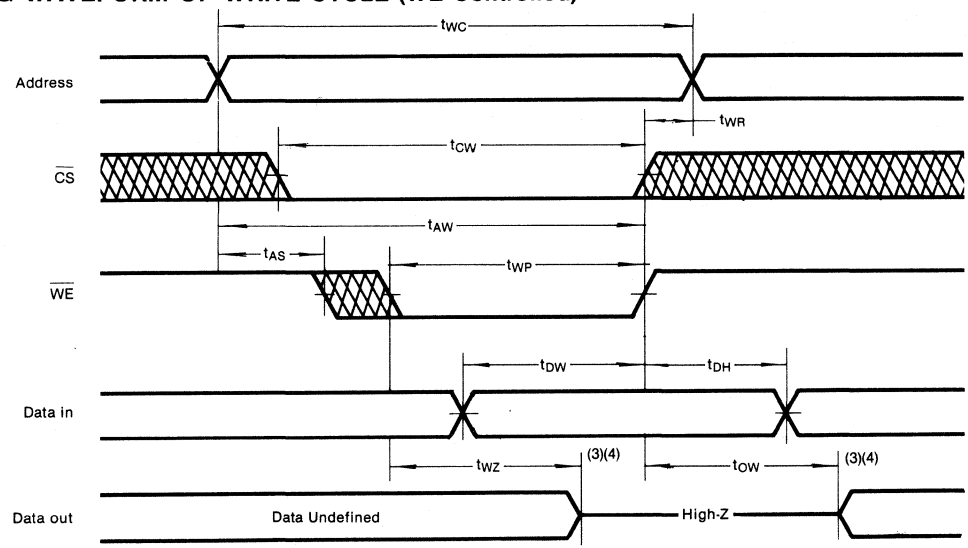
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



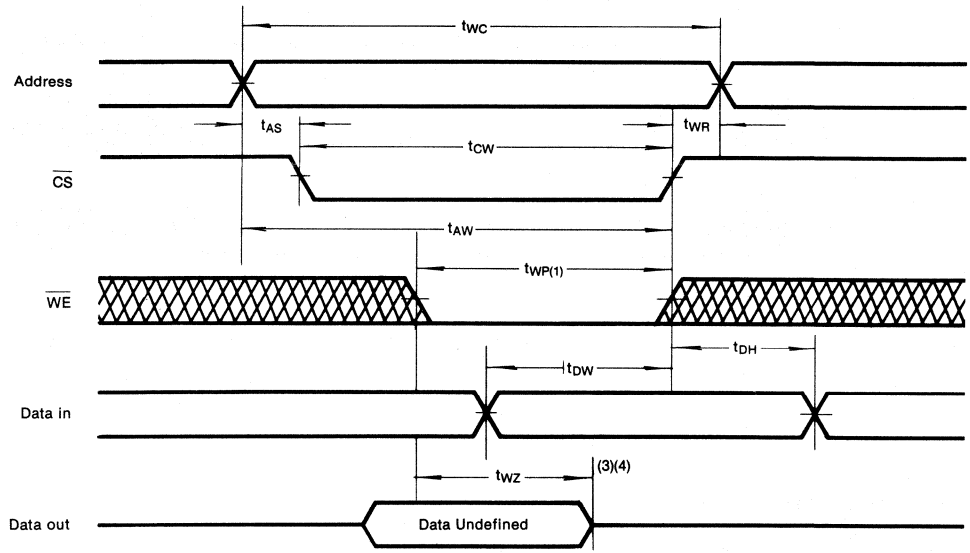
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or concident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	L	H	D_{OUT}	I_{CC}	Read
L	H	L	D_{IN}	I_{CC}	Write
L	L	L	D_{IN}	I_{CC}	Write

*Note: X means Don't Care.

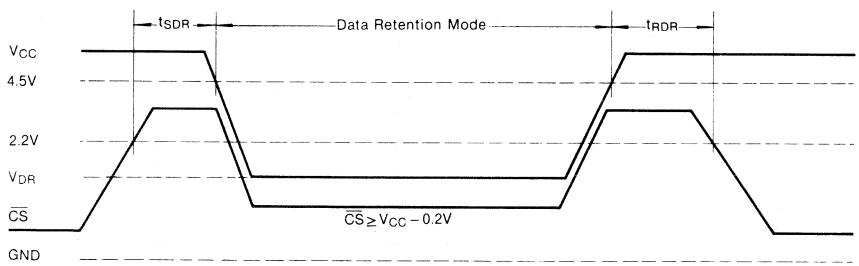
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(Guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1.0	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

*t_{RC} = Read Cycle Time

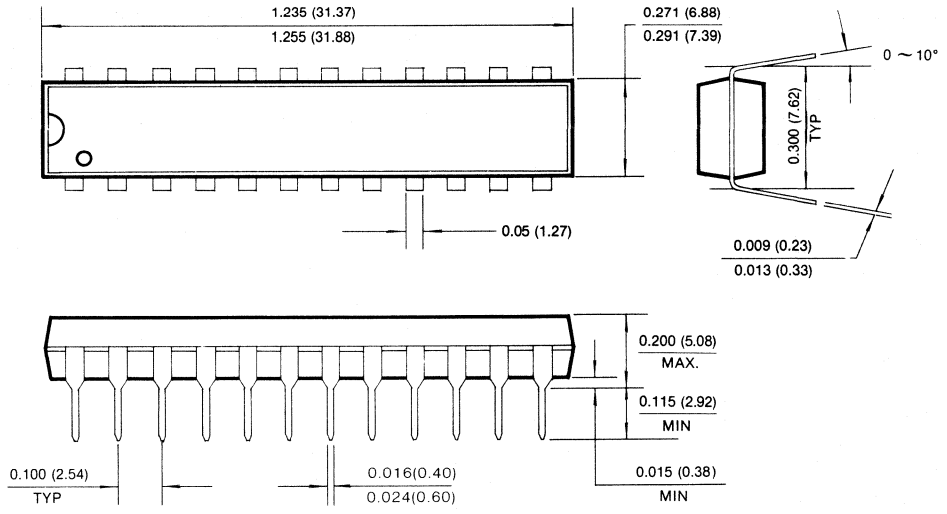
DATA RETENTION WAVEFORM



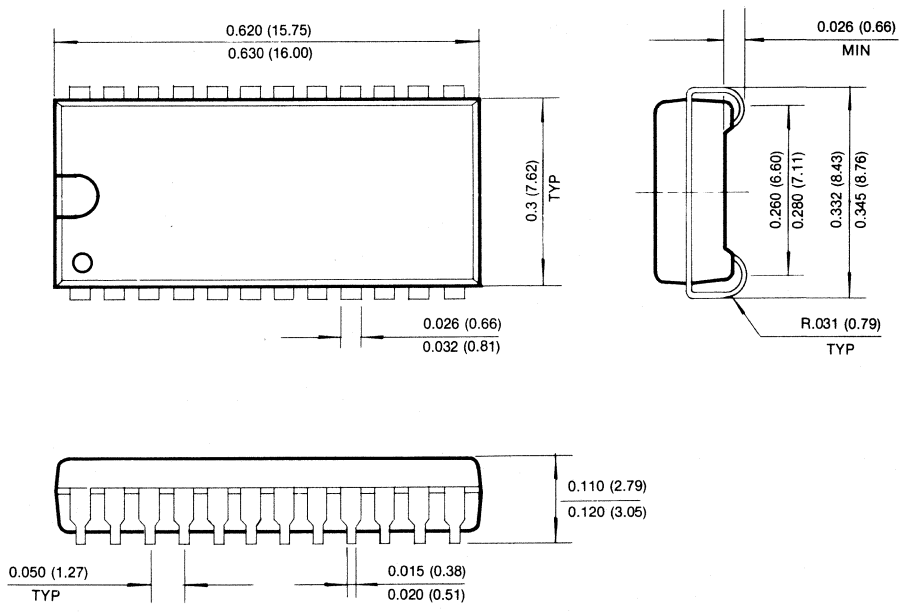
PACKAGE DIMENSIONS

24 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



24 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



16,384 WORD x 4 Bit CMOS Static RAM (With $\overline{OE}$)

FEATURES

- **Fast Access Time: 12, 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 35mA (max.)
  (CMOS): 1mA (max.)
  100μA (max.) L-Version
- **Operating KM6466BP/J-12: 140mA (max.)**
  KM6466BP/J-15: 130mA (max.)
  KM6466BP/J-20: 120mA (max.)
  KM6466BP/J-25: 110mA (max.)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  No clock or refresh required
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (min.)**
- **Standard 24-pin DIP (300 mil.), 24-pin SOJ (300 mil.)**

GENERAL DESCRIPTION

The KM6466B/BL is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bits.

The device is fabricated using Samsung's advanced CMOS process.

The KM6466B/BL has a chip select input for the minimum current power down mode.

The KM6466B/BL has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

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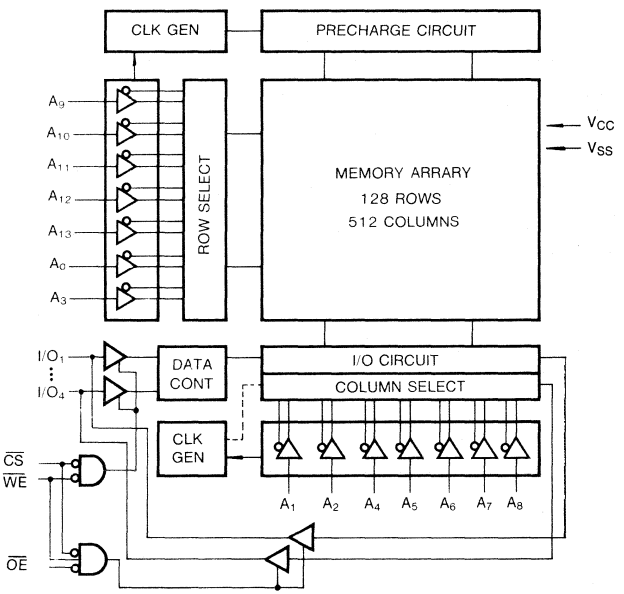
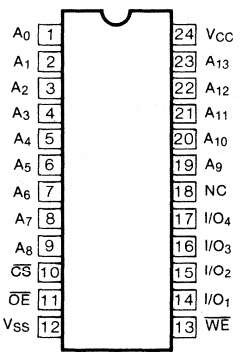
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}, V_{CC} = Max		—	—	1	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	12ns	—	110	140	mA
			15ns	—	95	130	mA
			20ns	—	85	120	mA
			25ns	—	75	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$		—	15	35	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$V		—	—	1	mA
			L		2	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

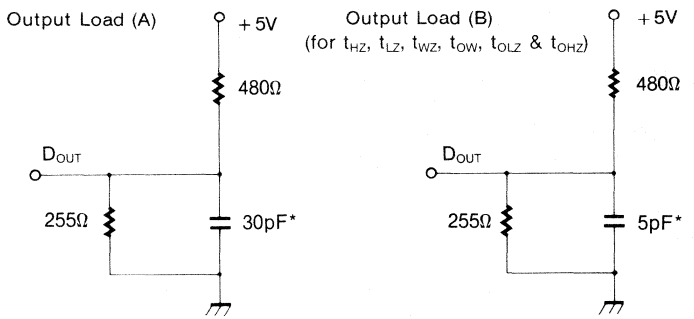
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6466BP-12 KM6466BJ-12		KM6466BP-15 KM6466BJ-15		KM6466BP-20 KM6466BJ-20		KM6466BP-25 KM6466BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AA}		12		15		20		25	ns
Chip Select to Output	t_{CO}		12		15		20		25	ns
Output Enable to Valid Output	t_{OE}		7		8		9		10	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		12		15		20		25	ns

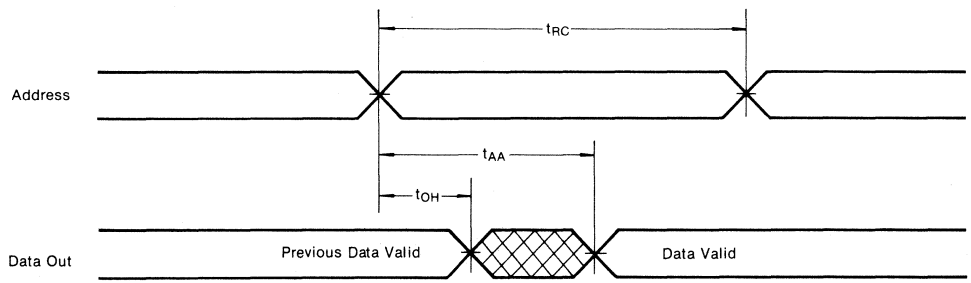
WRITE CYCLE

Parameter	Symbol	KM6466BP-12 KM6466BJ-12		KM6466BP-15 KM6466BJ-15		KM6466BP-20 KM6466BJ-20		KM6466BP-25 KM6466BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	10		12		13		15		ns
Write Pulse Width	t_{WP}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

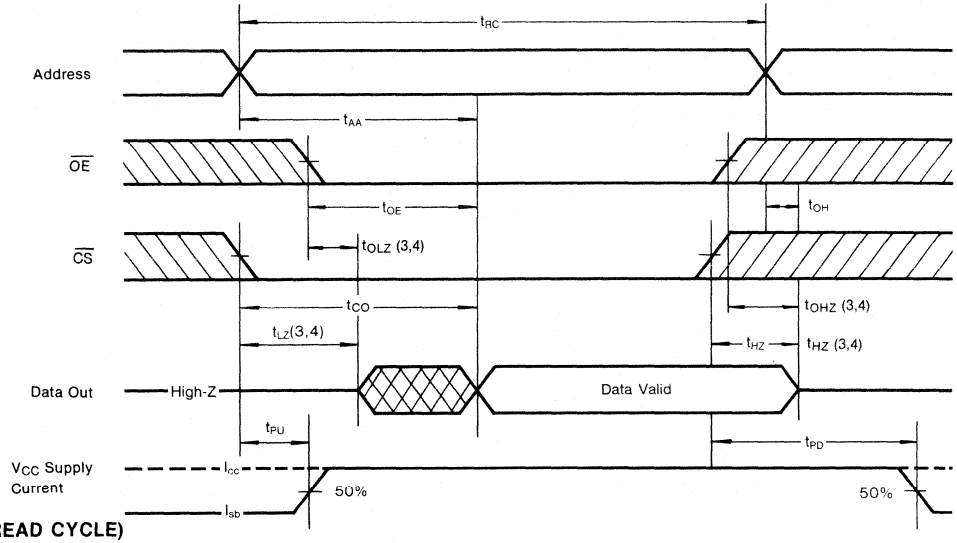
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS} = V_{IL}$, $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)



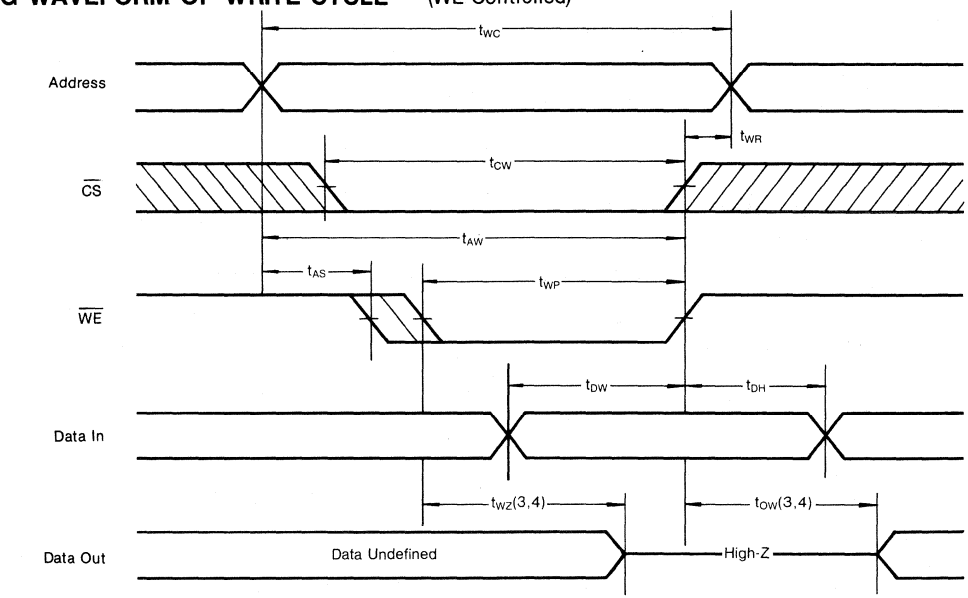
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



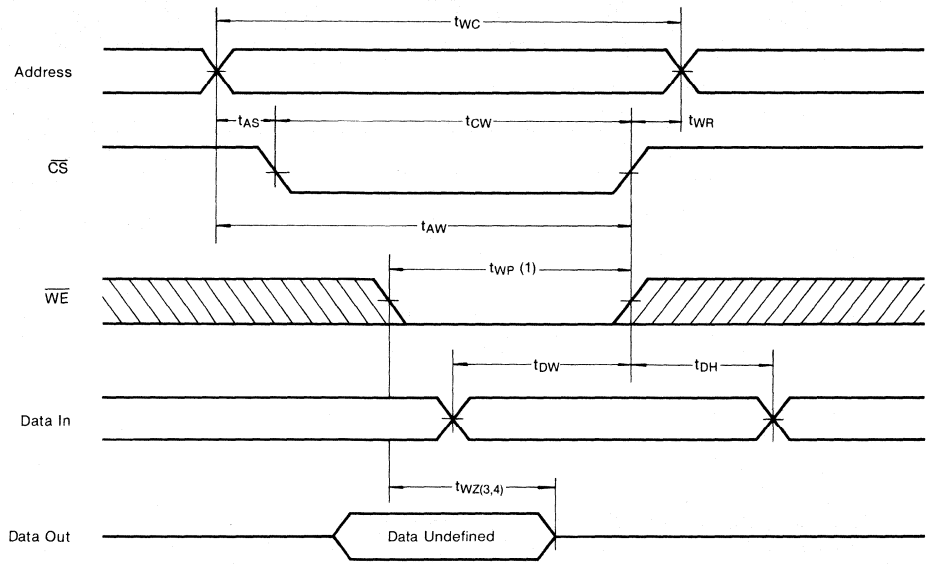
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.
7. $\overline{OE}$ is high for write cycle.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	L	D_{OUT}	I_{CC}	Read
L	L	X	D_{IN}	I_{CC}	Write

* Note: X means Don't Care.

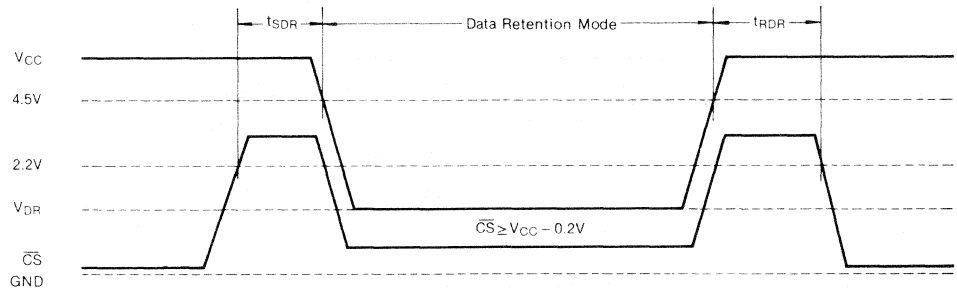
DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2		5.5	V
Data Retention Current	I_{DR}	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	50*	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}**			ns

*: V_{CC} = 3V
**: t_{RC} = Read Cycle Time

2

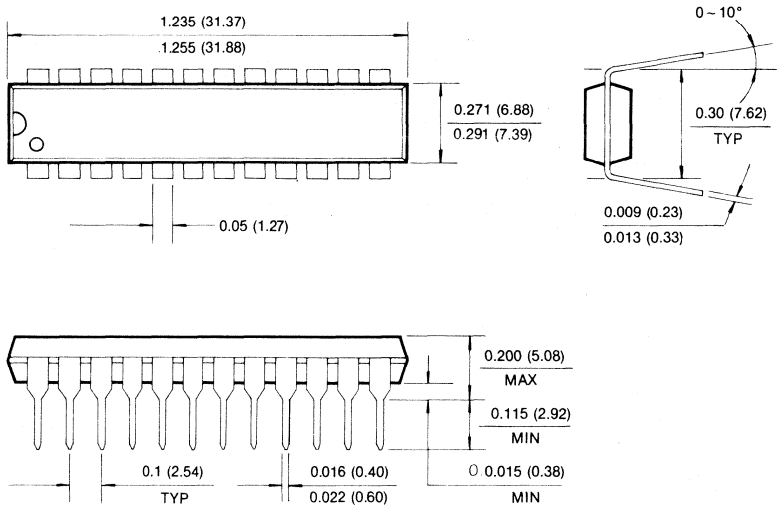
DATA RETENTION WAVEFORM



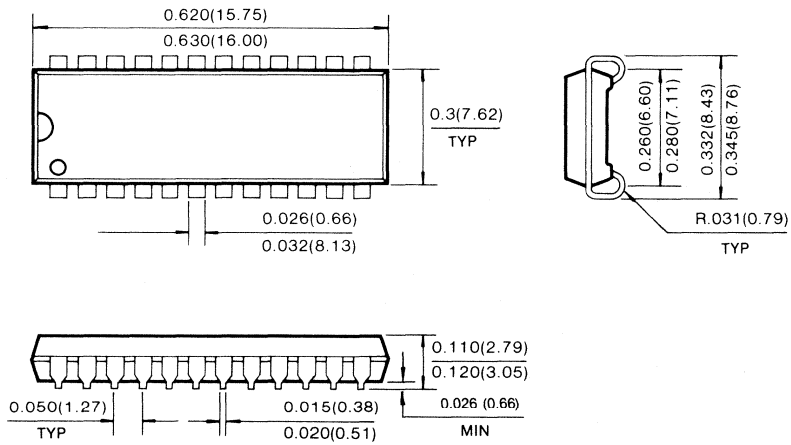
PACKAGE DIMENSIONS

24 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



24 PIN SMALL OUT LINE J FORM PACKAGE



8,192 WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 12, 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  Standby (TTL) : 35mA (max.)
  (CMOS): 1mA (max.)
  100μA (max.) L-Version
- **Operating KM6865BP/J-12: 140mA (max.)**
  KM6865BP/J-15: 130mA (max.)
  KM6865BP/J-20: 120mA (max.)
  KM6865BP/J-25: 110mA (max.)
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  No clock or refresh required
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (min.)**
- **Standard Pin Configuration**
  KM6865BP: 28-pin DIP (300 mil.)
  KM6865BJ: 28-pin SOJ (300 mil.)

GENERAL DESCRIPTION

The KM6865B/BL is a 65,536-bit high-speed Static Random Access Memory organized as 8,192 words by 8 bits.

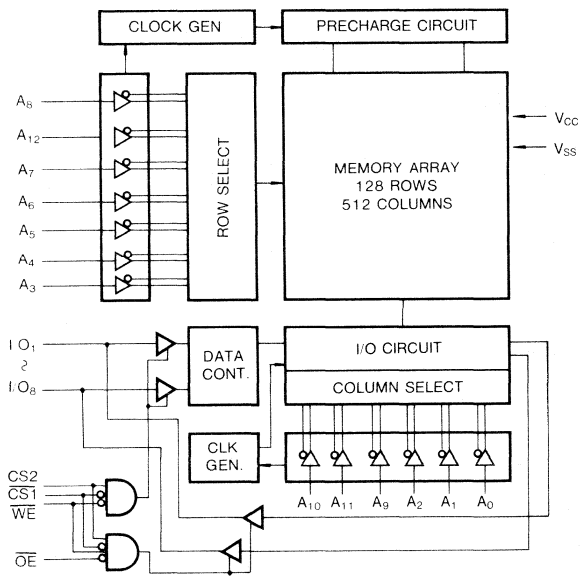
The KM6865B/BL uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications.

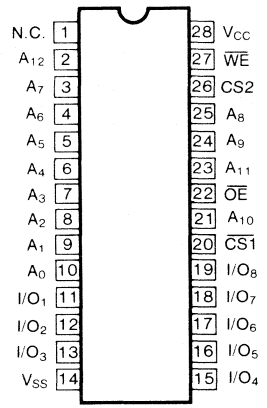
The KM6865B/BL is packaged in a 300 mil. 28-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Selects
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		—	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}, V_{CC} = Max		—	—	1	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, I_{OUT} = 0mA	12ns	—	110	140	mA
			15ns	—	95	130	mA
			20ns	—	85	120	mA
			25ns	—	75	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}		—	15	35	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{CC} − 0.2V, CS2 ≤ 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		—	—	1	mA
			L		2	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

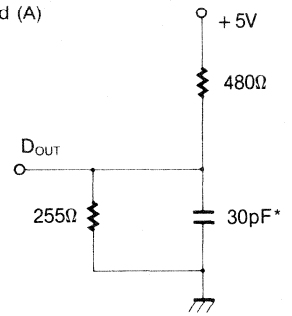
Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

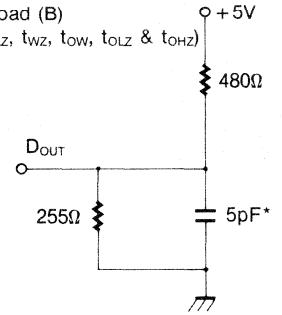
TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Loads	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6865BP-12 KM6865BJ-12		KM6865BP-15 KM6865BJ-15		KM6865BP-20 KM6865BJ-20		KM6865BP-25 KM6865BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AA}		12		15		20		25	ns
Chip Select to Output	t_{CO}		12		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		12		15		20		25	ns

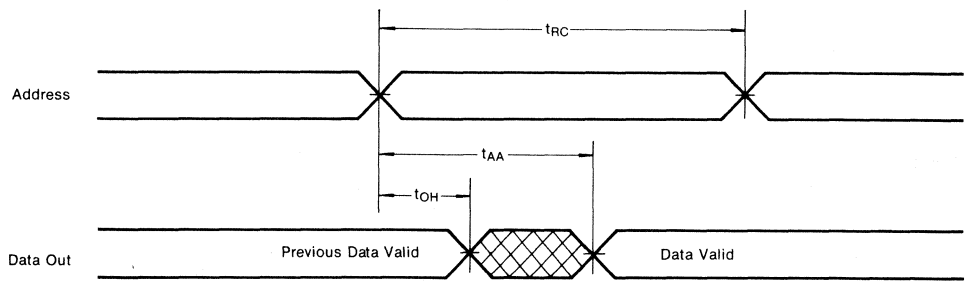
WRITE CYCLE

Parameter	Symbol	KM6865BP-12 KM6865BJ-12		KM6865BP-15 KM6865BJ-15		KM6865BP-20 KM6865BJ-20		KM6865BP-25 KM6865BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	10		12		13		15		ns
Write Pulse Width	t_{WP}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

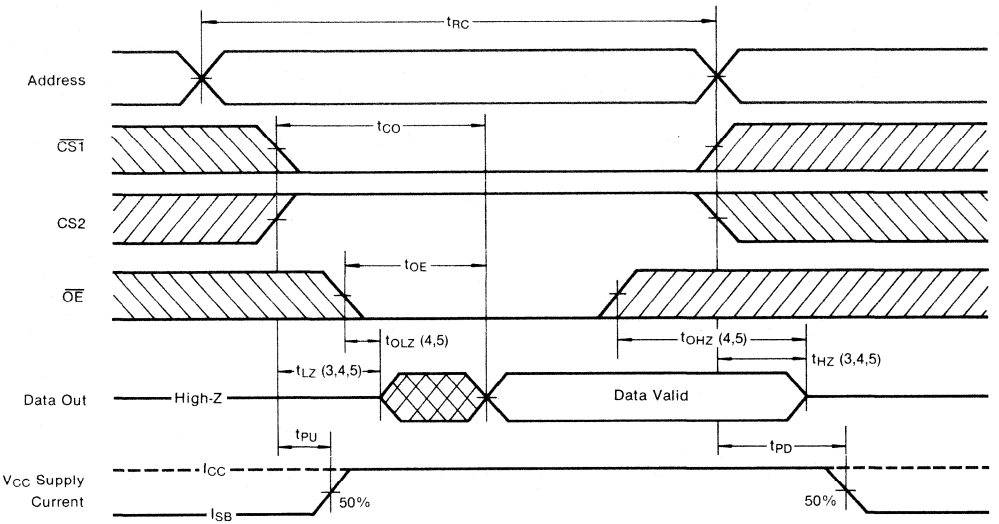
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}1 = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$)



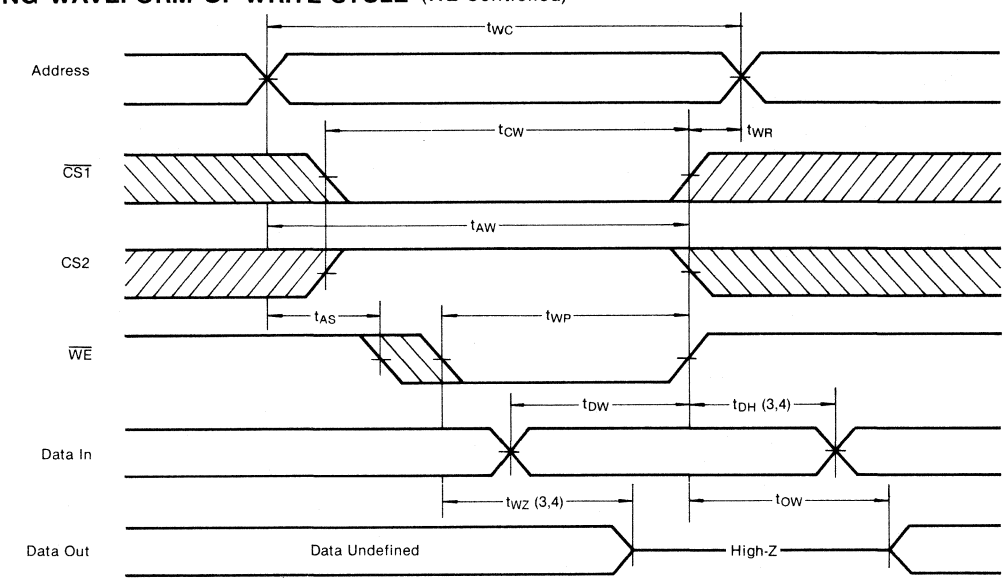
TIMING WAVEFORM OF READ CYCLE



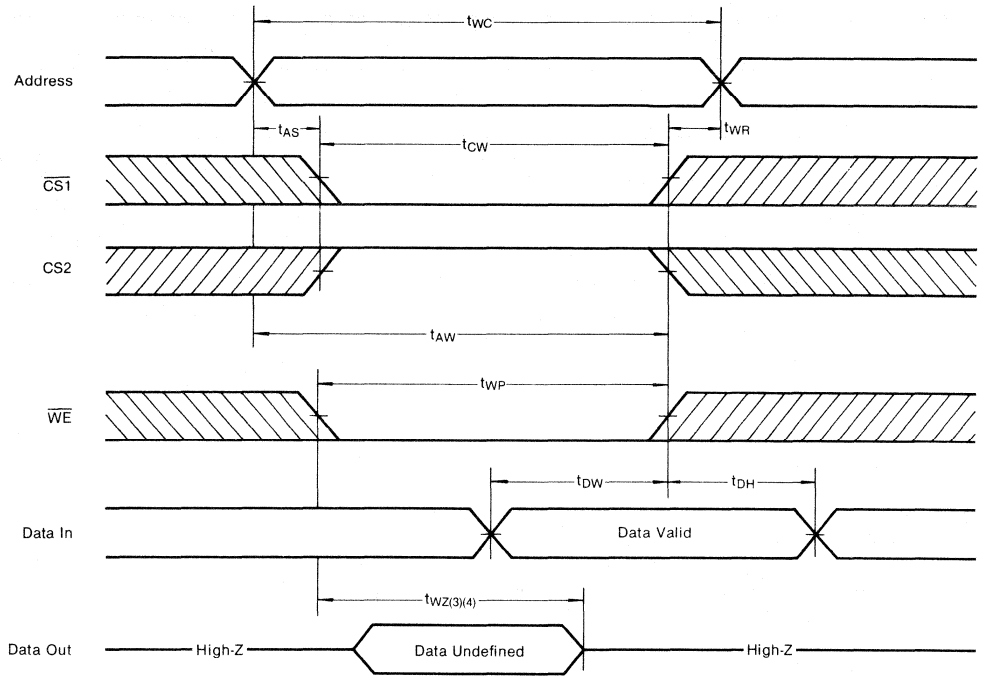
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ} (min) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, CS2 and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS1}$ or $\overline{WE}$ must be high or CS2 must be low during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

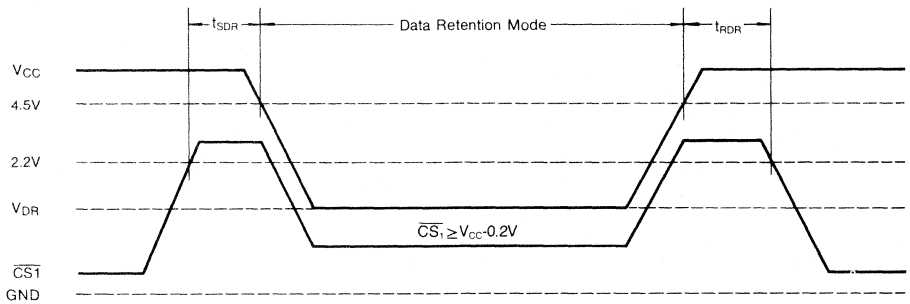
DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \leq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2		5.5	V
Data Retention Current	I_{DR}			1	50*	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}**			ns

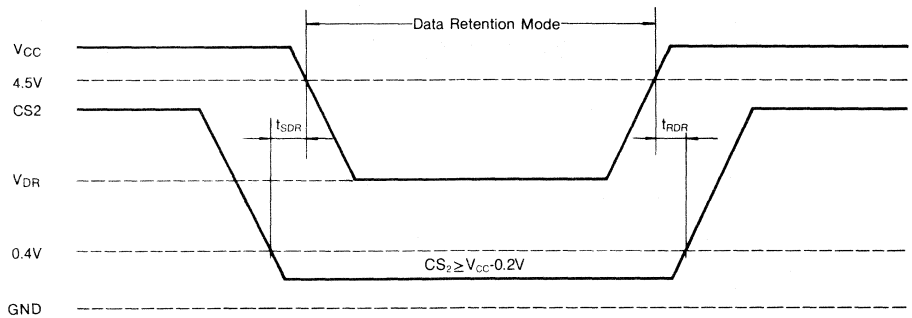
*: V_{CC} = 3V
**: t_{RC} = Read Cycle Time

2

DATA RETENTION WAVEFORM 1 ($\overline{CS1}$ Controlled)



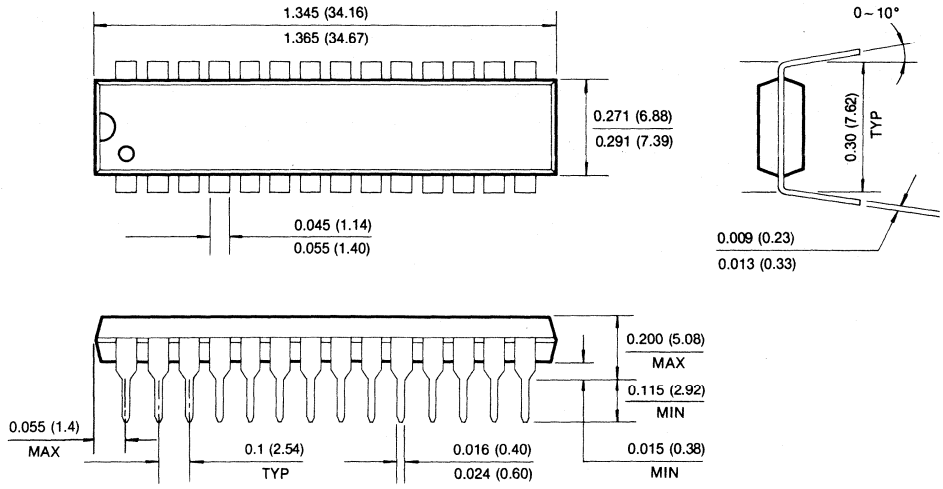
DATA RETENTION WAVEFORM 2 (CS2 Controlled)



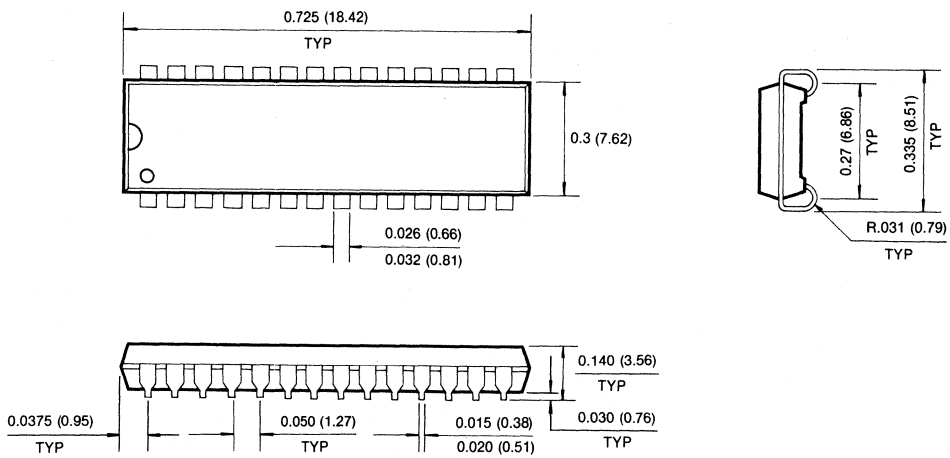
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



28 PIN SMALL OUT LINE J FORM PACKAGE



256K x 1 Bit Static RAM

FEATURES

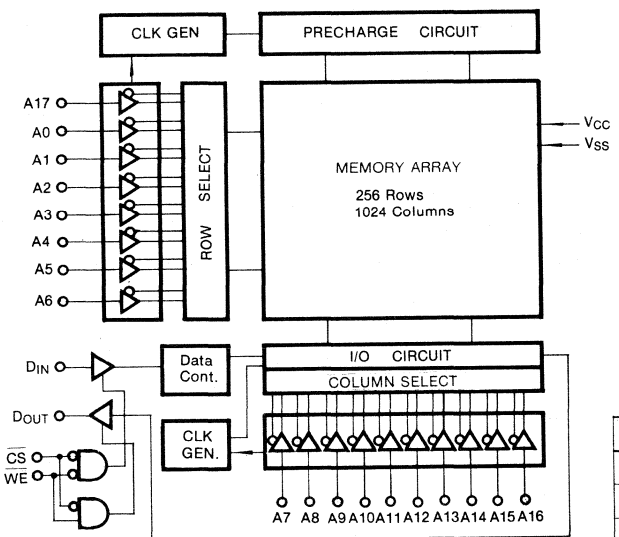
- Fast Access Time 25,35,45ns(max.)
- Low Power Dissipation
  - Standby (TTL) : 3 mA (max.)
  - (CMOS): 2mA (max.)
  - : 100μA (max.) L-Version
  - Operating : 100 mA (max.)
- Single 5V ± 10% Power Supply
- TTL compatible inputs and outputs
- Fully Static Operation
  - No clock or refresh required
- Three State Output
- Low Data Retention Current: 50 μA (max.)
- Battery Back-up Operation
  - 2V (min.) Data Retention
- Standard Pin Configuration
  KM61257AP/ALP: 24-pin DIP (300 mil.)
  KM61257AJ/ALJ: 24-pin SOJ (300 mil.)

GENERAL DESCRIPTION

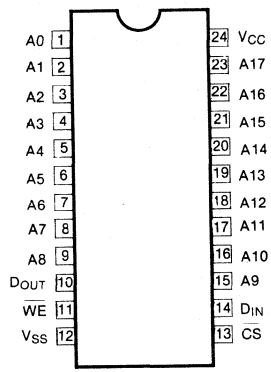
The KM61257A/AL is a 262,144-bit high-speed Static Random Access Memory organized as 262,144 words by 1 bit.
The device is fabricated using Samsung's advanced CMOS process.
The KM61257A/AL has a chip select input for the minimum current power down mode. The KM61257A/AL has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for non-volatility is required.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	0 to 70	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}*	−0.5	—	0.8	V

* $V_{IL}(min) = -3.0V$ for $\leq$20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{OUT} = V_{SS}$ to V_{CC}			2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = 0mA$			20	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, $I_{OUT} = 0mA$			100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$			2	mA
			L		100	μA
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0V$	—	7	pF

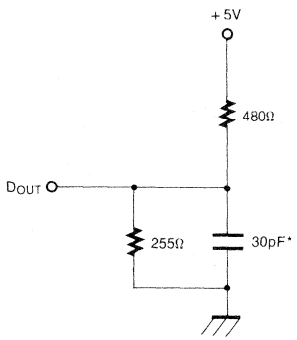
*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

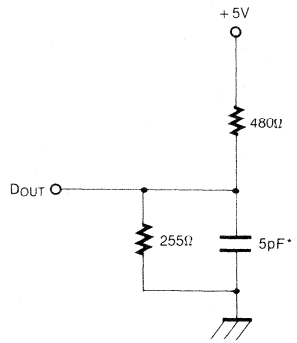
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM61257A-25 KM61257AL-25		KM61257A-35 KM61257AL-35		KM61257A-45 KM61257AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{CO}		25		35		45	ns
Chip Select to Low-Z Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		20		30		30	ns

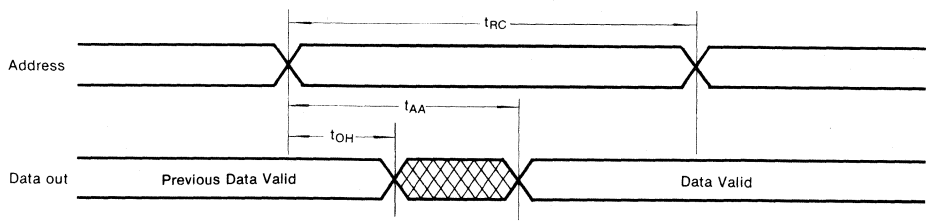
WRITE CYCLE

Parameter	Symbol	KM61257A-25 KM61257AL-25		KM61257A-35 KM61257AL-35		KM61257A-45 KM61257AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		40		ns
Chip Select to End of Write	t_{CW}	25		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	25		30		40		ns
Write Pulse Width	t_{WP}	25		25		35		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	15	0	20	0	20	ns
Data to Write Time Overlap	t_{DW}	15		20		25		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

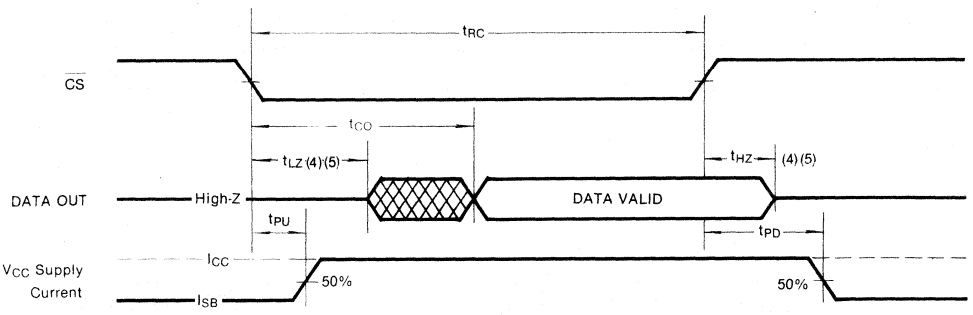
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH})



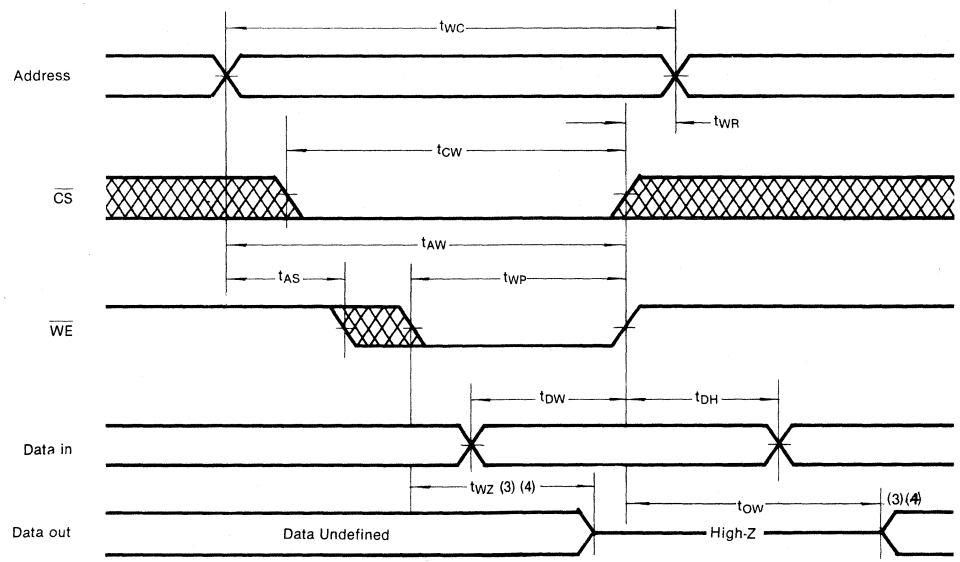
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



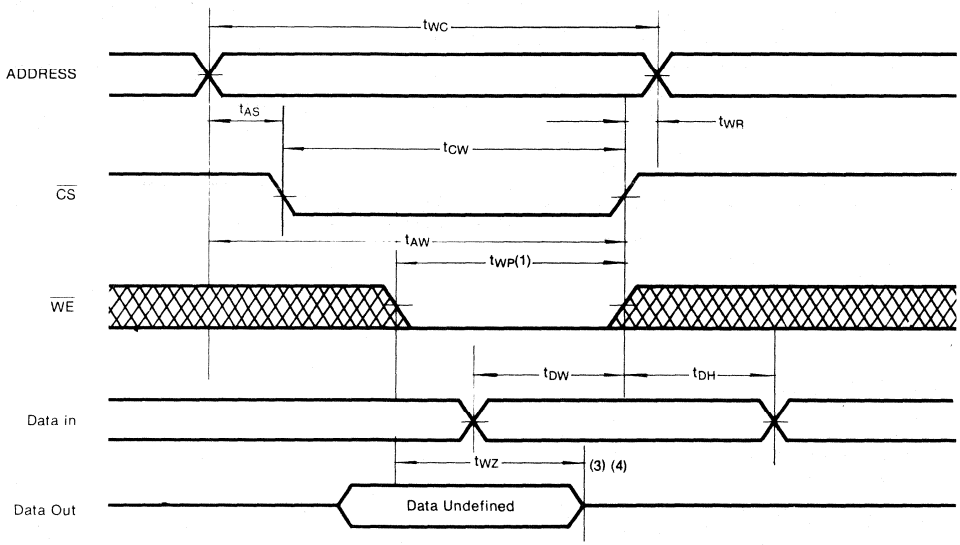
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	D_{OUT} PIN	Supply Current	Mode
H	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	L	D_{IN}	I_{CC1}, I_{CC2}	Write

*Note: X means Don't Care.

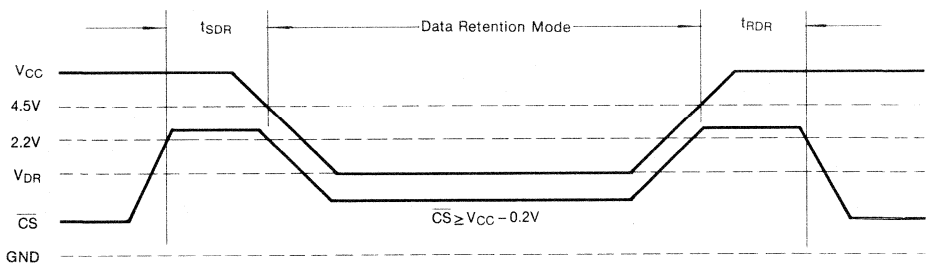
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(Guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1.0	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

*t_{RC} = Read Cycle Time

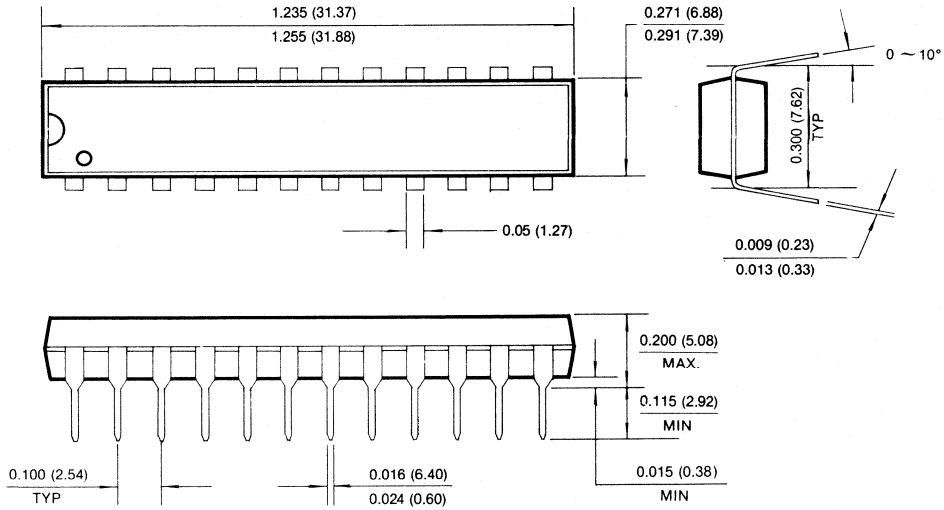
DATA RETENTION WAVEFORM



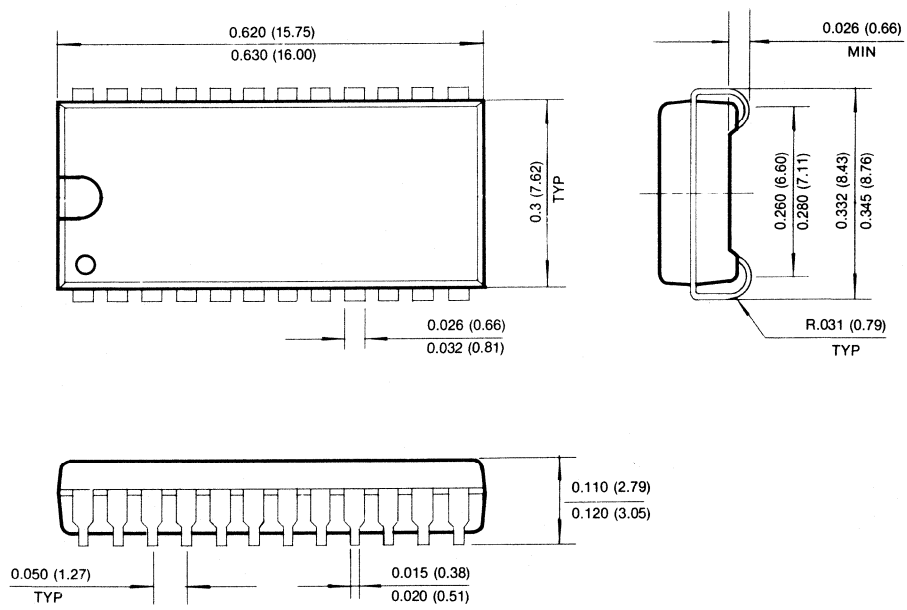
PACKAGE DIMENSIONS

24 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



24 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



64K x 4 Bit Static RAM

FEATURES

- Fast Access Time 25,35,45ns(max.)
- Low Power Dissipation
  - Standby (TTL) : 3 mA (max.)
  - (CMOS): 2mA (max.)
  - 100μA (max.) L-Version
  - Operating : 120 mA (max.)
- Single 5V $\pm$ 10% Power Supply
- TTL compatible inputs and outputs
- Fully Static Operation
  - No clock or refresh required
- Three State Output
- Low Data Retention Current: 50 μA (max.)
- Battery Back-up Operation
  - 2V (min.) Data Retention
- Standard Pin Configuration
  KM64257AP/ALP: 24-pin DIP (300 mil.)
  KM64257AJ/ALJ: 24-pin SOJ (300 mil.)

GENERAL DESCRIPTION

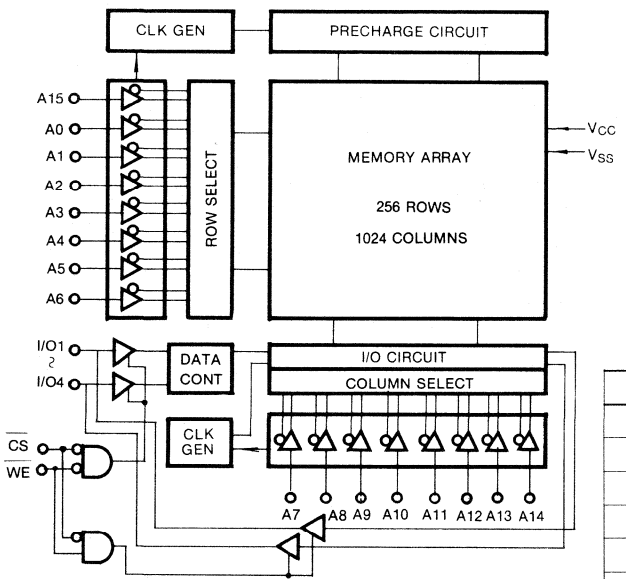
The KM64257A/AL is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bit.

The device is fabricated using Samsung's advanced CMOS process.

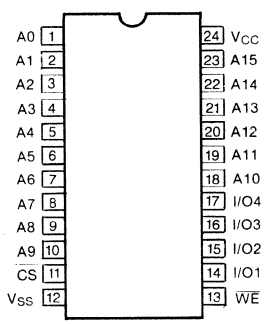
The KM64257A/AL has a chip select input for the minimum current power down mode. The KM64257A/AL has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for non-volatility is required.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	0 to 70	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{OUT} = V_{SS}$ to V_{CC}			2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH} $I_{I/O}$ = 0mA			20	mA
Average Operating Current	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$			2	mA
			L		100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA		2.4		V

CAPACITANCE (f = 1MHz, Ta = 25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

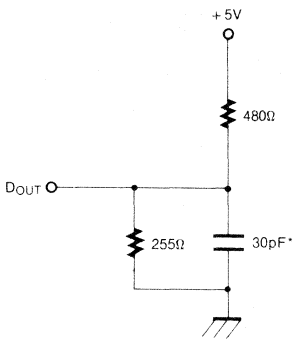
*Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

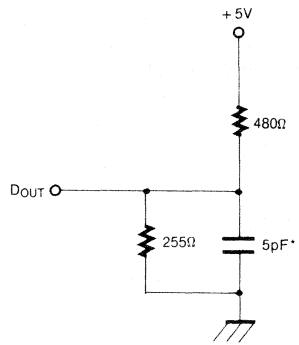
TEST CONDITIONS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.5V
Output Load	See below

Output Load(a)



Output Load(b)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64257A-25 KM64257AL-25		KM64257A-35 KM64257AL-35		KM64257A-45 KM64257AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		ns
Address Access Time	t_{AA}		25		35		45	ns
Chip Select to Output	t_{CO}		25		35		45	ns
Chip Select to Low-Z Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	15	0	15	0	20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		20		30		30	ns

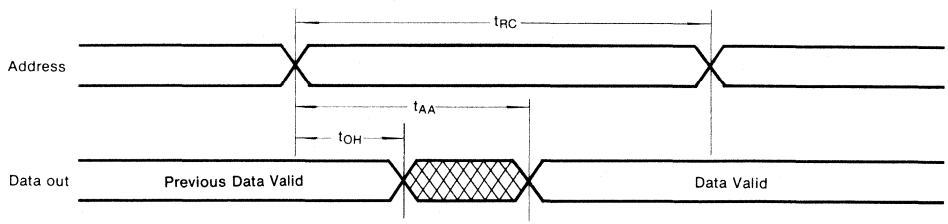
WRITE CYCLE

Parameter	Symbol	KM64257A-25 KM64257AL-25		KM64257A-35 KM64257AL-35		KM64257A-45 KM64257AL-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		30		40		ns
Chip Select to End of Write	t_{CW}	25		30		40		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	25		30		40		ns
Write Pulse Width	t_{WP}	25		30		35		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	15	ns
Data to Write Time Overlap	t_{DW}	17		20		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

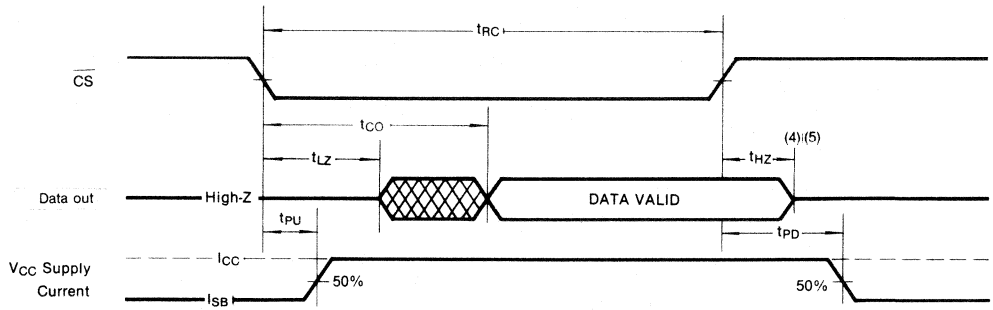
TIMING DIAGRAMS

READ CYCLE TIMING (Address Controlled)

($\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH})



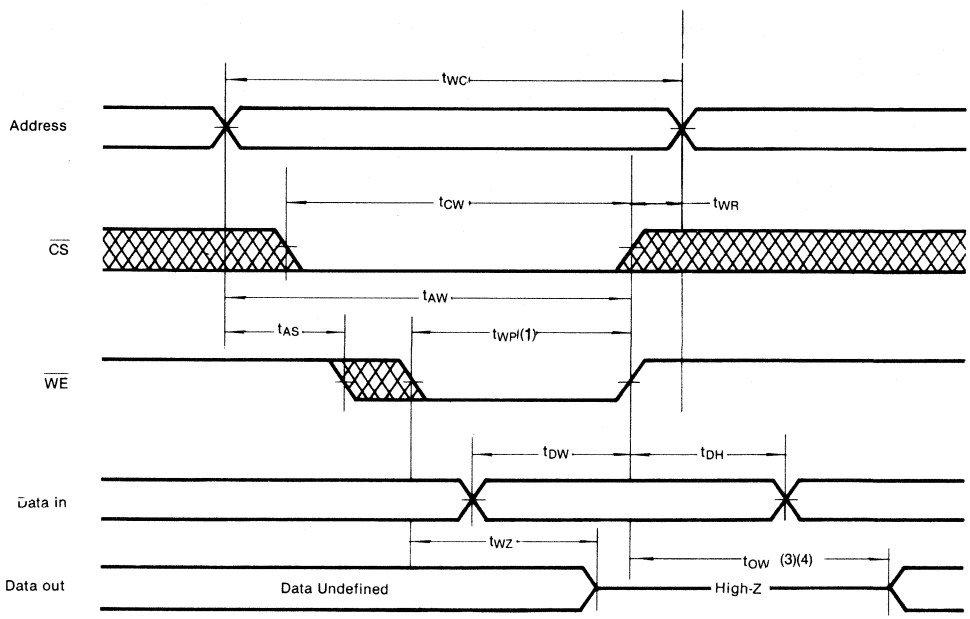
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



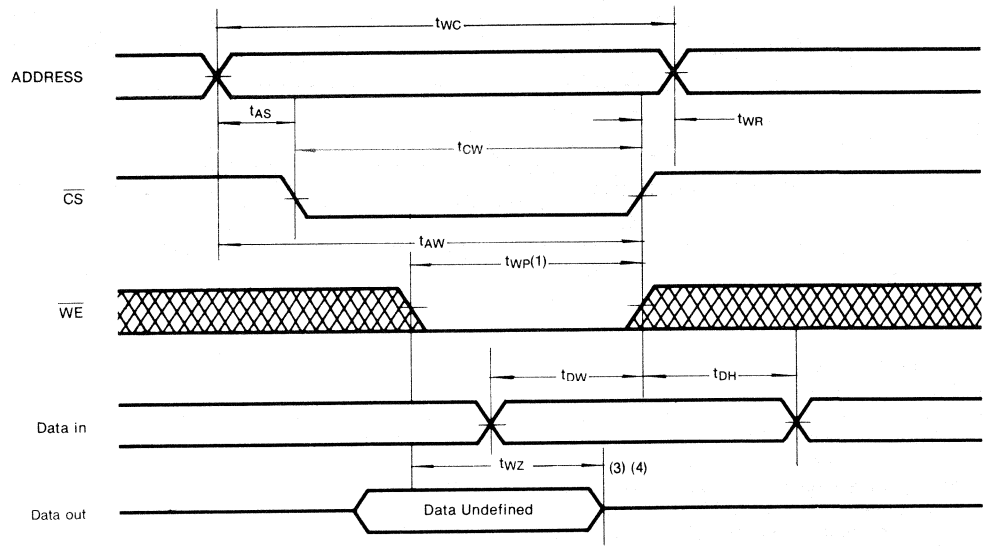
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(b).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

WRITE CYCLE TIMING ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(b).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	I/O PIN	Supply Current	Mode
H	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	L	D_{IN}	I_{CC1}, I_{CC2}	Write

*Note: X means Don't Care.

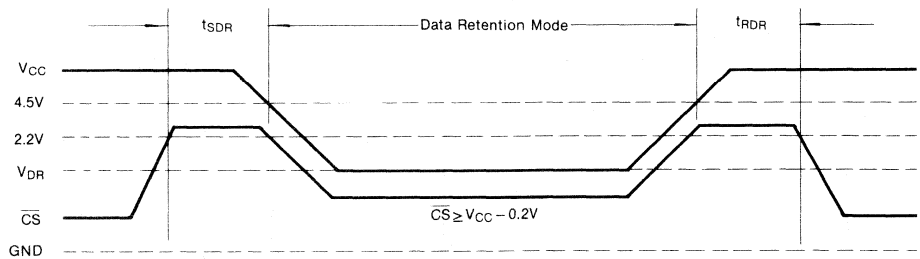
DATA RETENTION CHARACTERISTICS (Ta = 0 to 70°C)

(Guaranteed only for L-version)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$		1.0	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}*			ns

*t_{RC} = Read Cycle Time

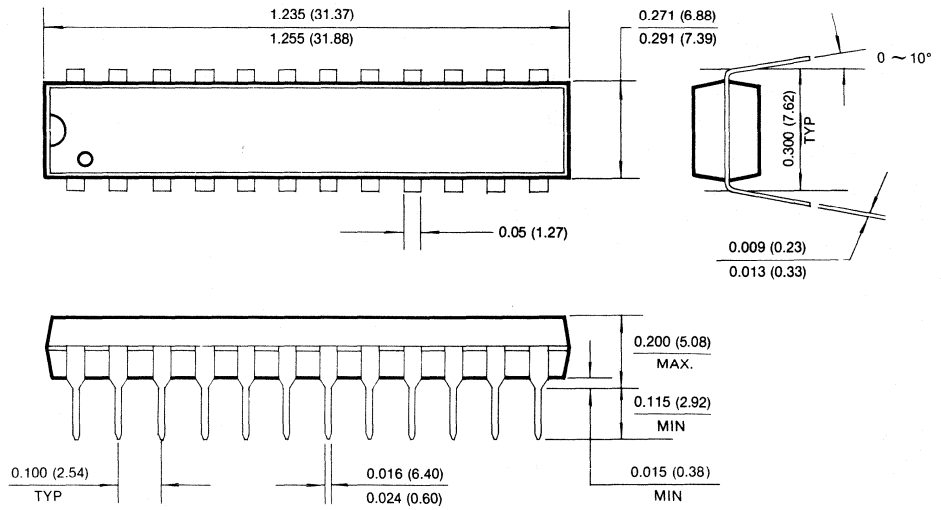
DATA RETENTION WAVEFORM



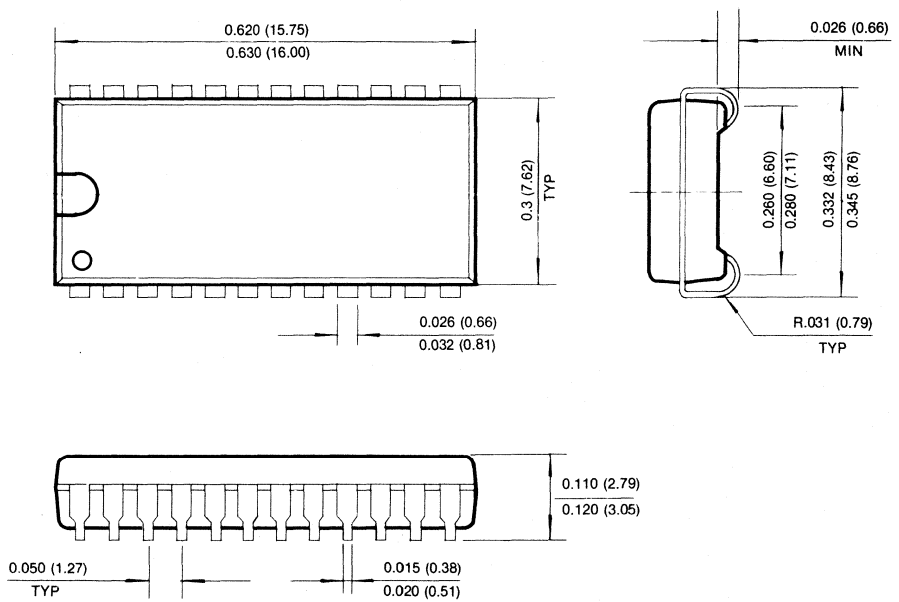
PACKAGE DIMENSIONS

24 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



24 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



64KX4 Bit High-Speed CMOS Static RAM (With $\overline{OE}$)

FEATURES

- **Fast Access Time: 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS): 2mA (max)**
  - **Operating KM64257BP/J-15: 140mA (max.)**
  - **KM64257BP/J-20: 130mA (max.)**
  - **KM64257BP/J-25: 120mA (max.)**
- **Single 5V±10% Power Supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three state Outputs**
- **Standard Pin Configuration**
  - **KM64258BP: 28-pin DIP (300 mil.)**
  - **KM64258BJ: 28-pin SOJ (300 mil.)**

GENERAL DESCRIPTION

The KM64258B is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

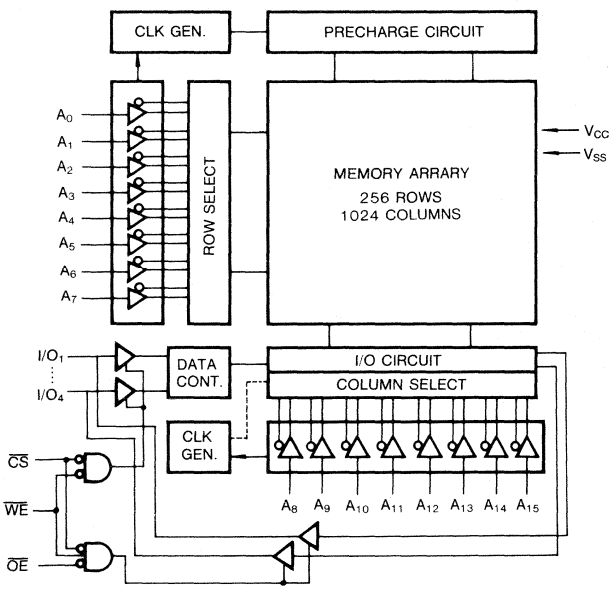
The KM64258B uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

It is particularly well suited for use in high-density high-speed system applications.

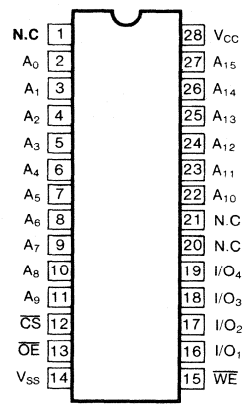
The KM64258B is packaged in a 300 mil 28-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ≤10ns pulse.

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}				2	μA
Output Leakge Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}				2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	15ns			140	mA
			20ns			130	mA
			25ns			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}				40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}−0.2V, V_{IN}≥V_{CC}−0.2V or V_{IN}≤0.2V				2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA		2.4			V

* Typ: V_{CC}=5V, T_A=25°C

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

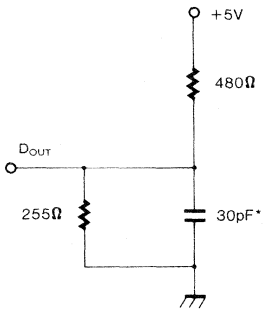
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

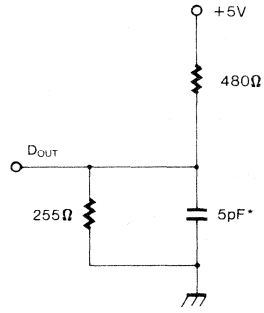
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B) (for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64258BP-15 KM64258BJ-15		KM64258BP-20 KM64258BJ-20		KM64258BP-25 KM64258BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		20		25	ns

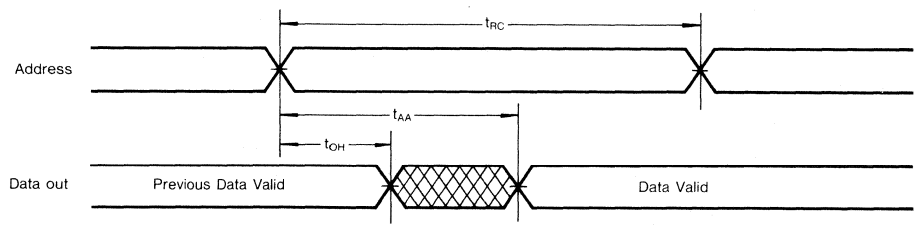
WRITE CYCLE

Parameter	Symbol	KM64258BP-15 KM64258BJ-15		KM64258BP-20 KM64258BJ-20		KM64258BP-25 KM64258BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	9		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

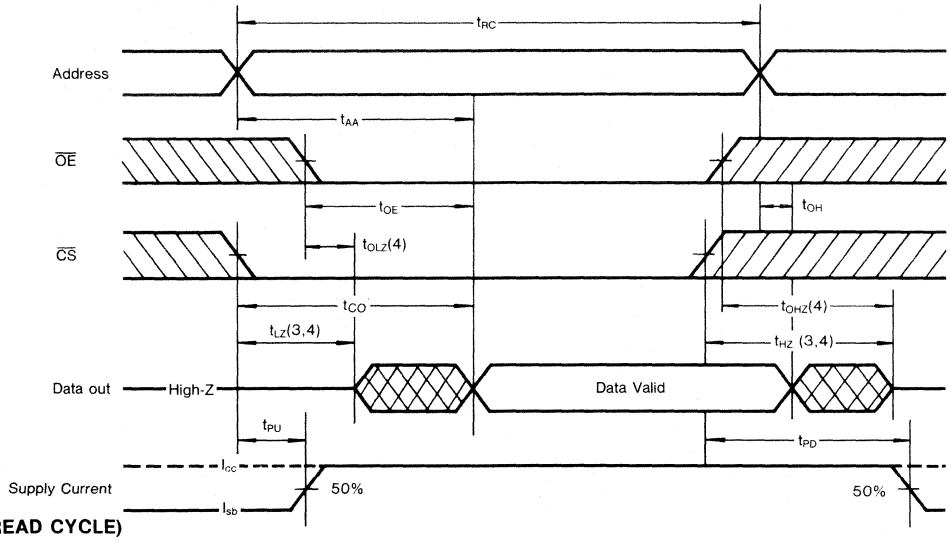
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



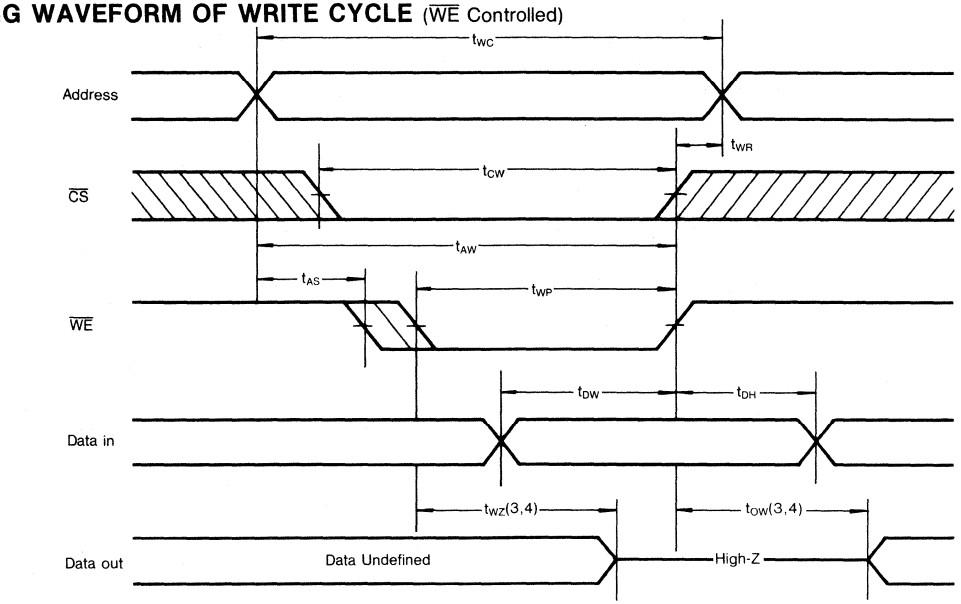
TIMING WAVEFORM OF READ CYCLE



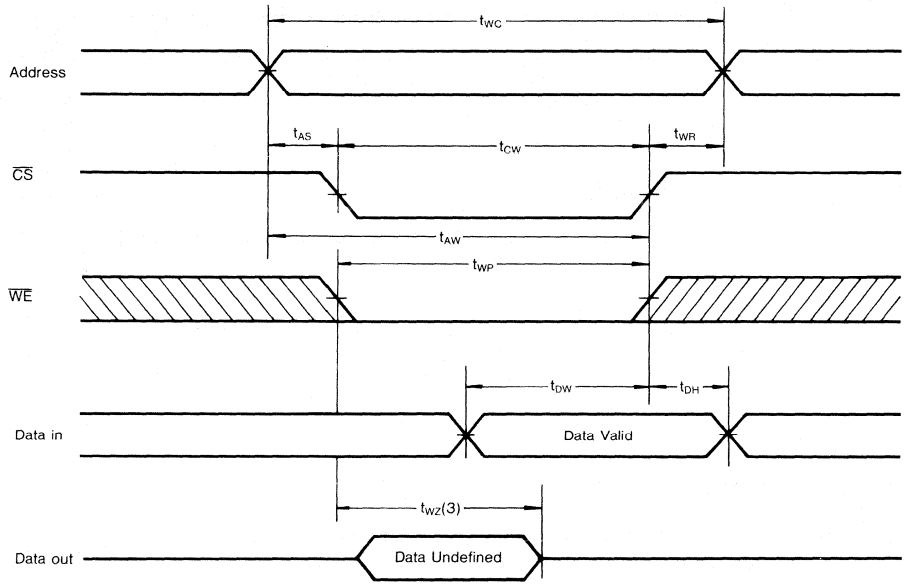
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

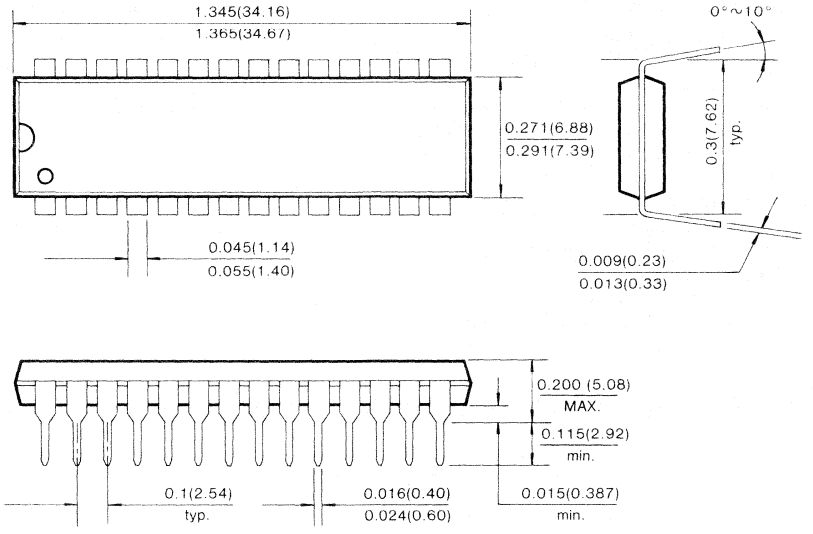
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care

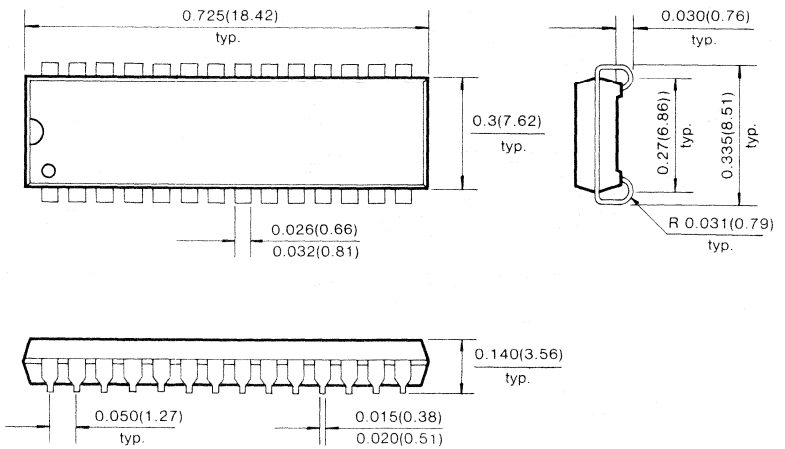
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



65,536 WORD × 4 Bit (With $\overline{OE}$) High-Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 10, 12ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 90mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM64B258AJ-8: 185mA (max.)**
  - **KM64B258AJ-10: 175mA (max.)**
  - **KM64B258AJ-12: 165mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM64B258AJ: 28-pin SOJ (300 mil)**

GENERAL DESCRIPTION

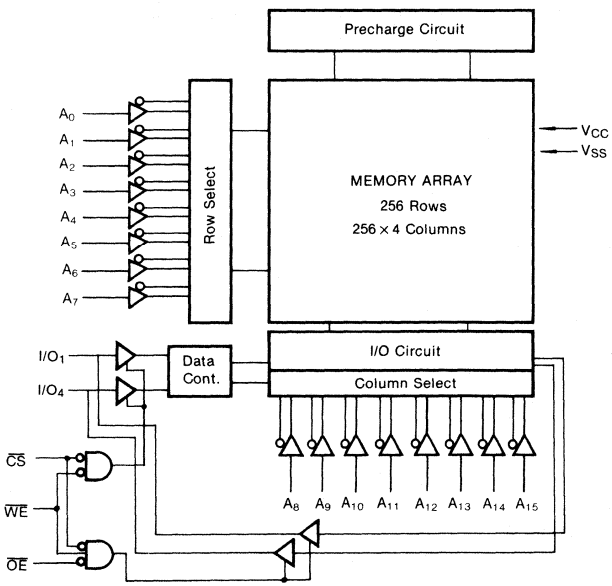
The KM64B258A is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

The KM64B258A uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology.

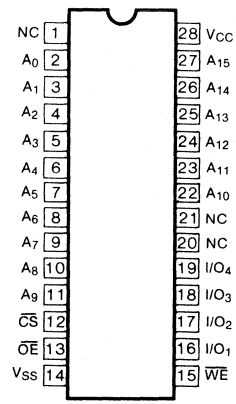
It is particularly well suited for use in high-density high-speed system applications.

The KM64B258A is packaged in a 300 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.)=−2.0V ac (pulse width ≤ 8ns) for I ≤ 20mA
** V_{IH} (max.)=V_{CC}+2V ac (pulse width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = V_{SS} to V_{CC}		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	8ns	—	185	mA
			10ns	—	175	mA
			12ns	—	165	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL}, Min. Cycle		—	90	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		—	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note: Capacitance is sampled and not 100% tested.

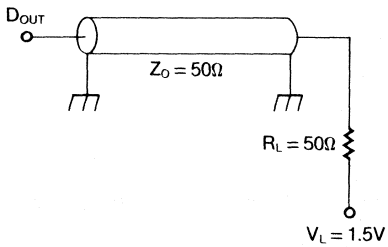
AC CHARACTERISTICS

TEST CONDITIONS

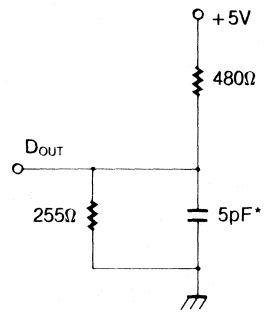
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64B258A-8		KM64B258A-10		KM64B258A-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8		10		12		ns
Address Access Time	t_{AA}		8		10		12	ns
Chip Select to Output	t_{CO}		8		10		12	ns
Output Enable to Valid Output	t_{OE}		4		5		7	ns
Chip Enable to Low-Z Output	t_{LZ}	4		4		4		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	4		4		4		ns

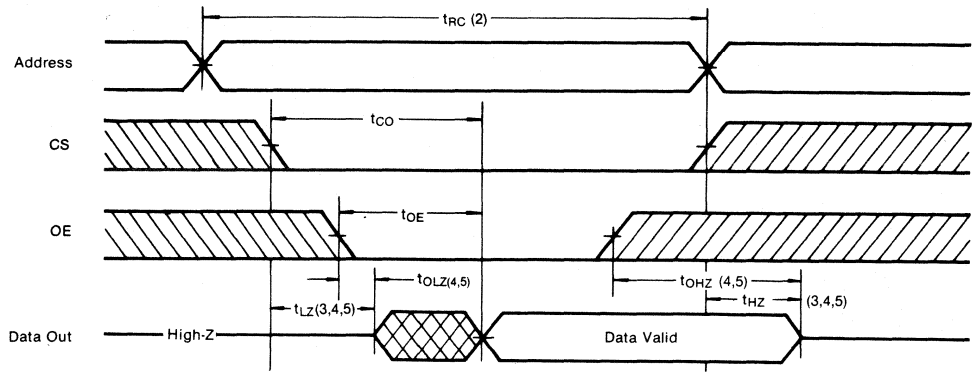
WRITE CYCLE

Parameter	Symbol	KM64B258A-8		KM64B258A-10		KM64B258A-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8		10		12		ns
Chip Select to End of Write	t_{CW}	6		7		9		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	8		9		10		ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6		7		9		ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8		10		12		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4		5		6		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	4		4		4		ns

2

TIMING DIAGRAMS

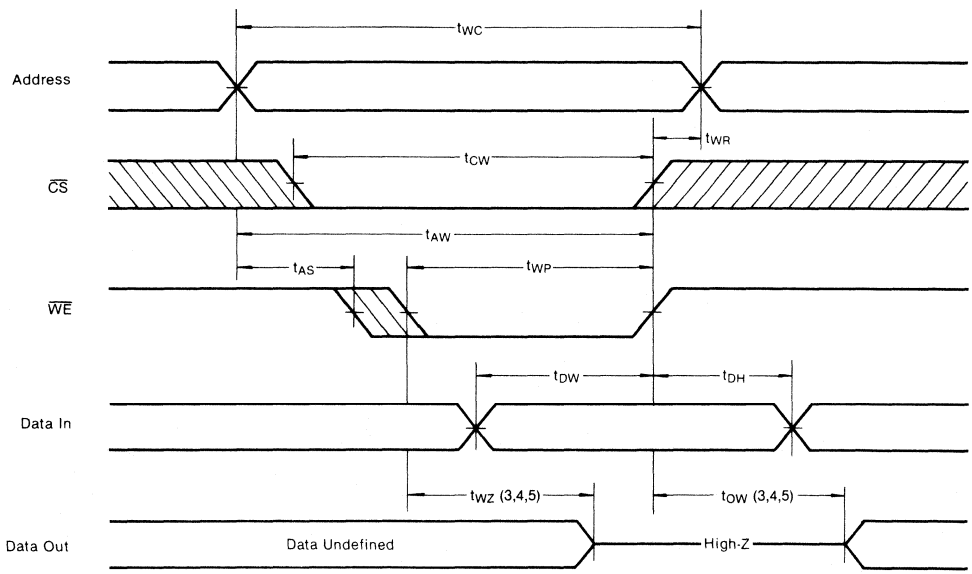
TIMING WAVEFORM OF READ CYCLE



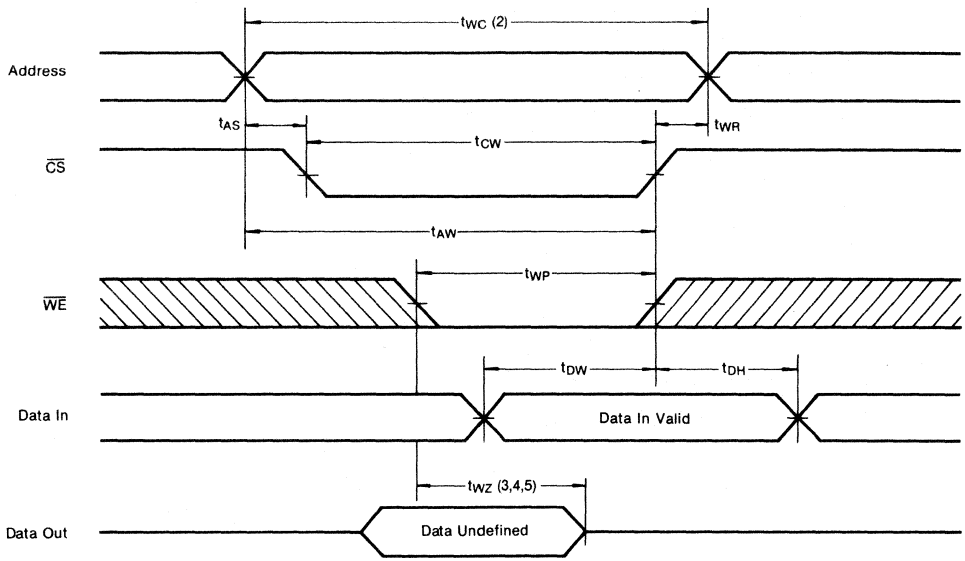
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.

FUNCTIONAL DESCRIPTION

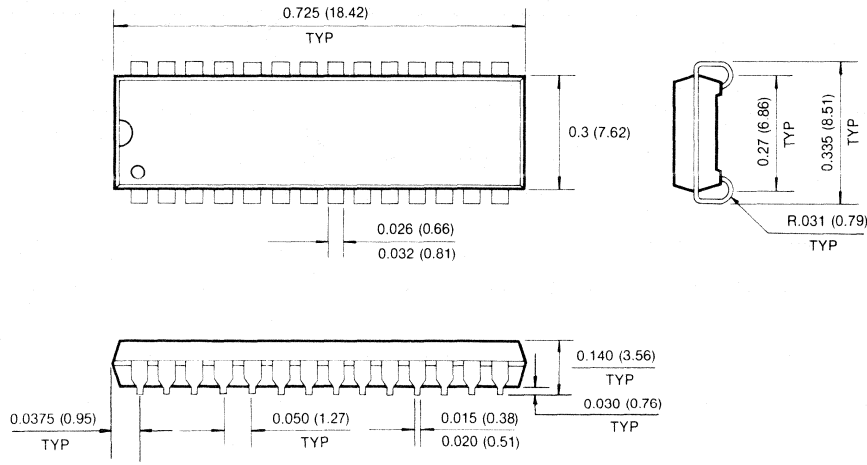
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

PACKAGE DIMENSIONS

28 PIN SMALL OUT LINE J FORM PACKAGE

Unit: Inches (millimeters)



64KX4 Bit High-Speed CMOS Static RAM (Sep. I/O)

FEATURES

- Fast Access Time: 15, 20, 25ns (max.): KM64259B
  20, 25ns (max.): KM64260B
- Low Power Dissipation
  Standby (TTL) : 40mA (max.)
  (CMOS): 2mA (max.)
  Operating: -15ns: 140mA (max.): KM64259B only
  20ns: 130mA (max.)
  25ns: 120mA (max.)
- **Single 5V±10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  —No clock or refresh required
- **Three State Outputs**
- **Standard Pin Configuration**
  KM64259BP/KM64260BP: 28-pin DIP (300 mil.)
  KM64259BJ/KM64260BJ: 28-pin SOJ (300 mil.)

GENERAL DESCRIPTION

The KM64259B and KM64260B are a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits.

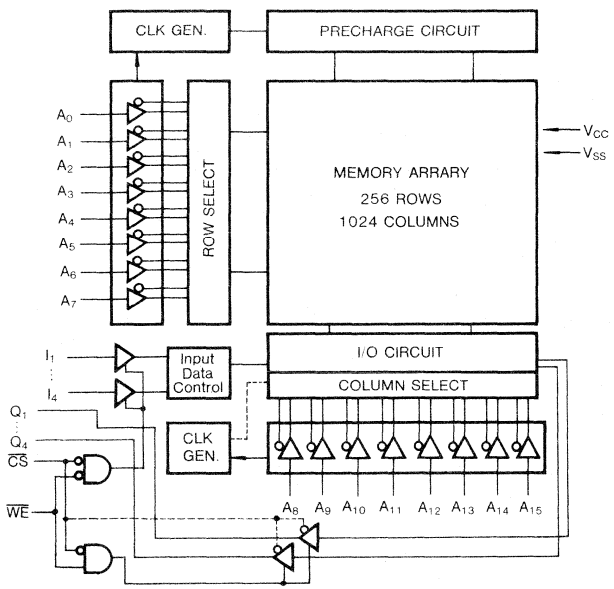
The KM64259B and KM64260B have seperate input and output lines for fast read and write access. The data output pins stay in High-Z state when write enable is low (KM64259B only), or chip select is high.

The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

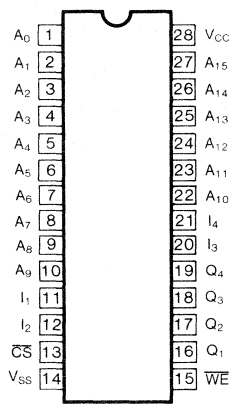
It is particularly well suited for use in high-density high-speed system applications.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{15}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$I_1 \sim I_4$	Data Inputs
$Q_1 \sim Q_4$	Data Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}				2	μA
Output Leakge Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}				2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	15ns			140	mA
			20ns			130	mA
			25ns			120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}				40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}−0.2V, V_{IN}≥V_{CC}−0.2Vor V_{IN}≤0.2V				2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA		2.4			V

* Typ: V_{CC}=5V, T_A=25°C

CAPACITANCE* (f=1MHz, T_A=25°C)

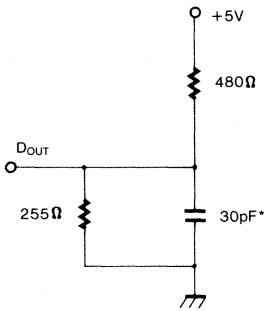
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	7	pF

AC CHARACTERISTICS

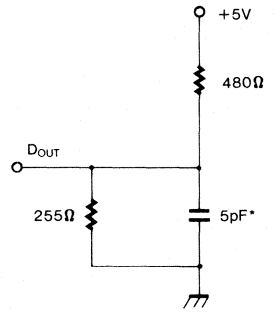
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WHZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64259BP/J-15		KM64259BP/J-20 KM64260BP/J-20		KM64259BP/J-25 KM64260BP/J-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		20		25	ns

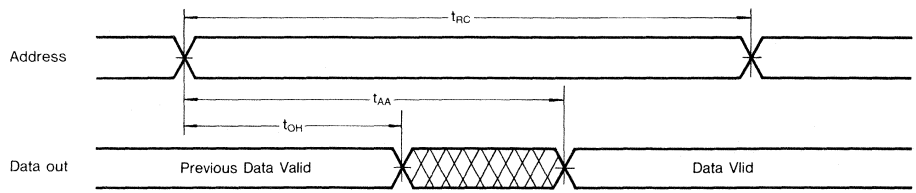
WRITE CYCLE

Parameter	Symbol	KM64259BP/J-15		KM64259BP/J-20 KM64260BP/J-20		KM64259BP/J-25 KM64260BP/J-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data to Write Time Overlap	t_{DW}	8		10		13		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Write to Output High-Z (KM64259B)	t_{WHZ}	0	8	0	9	0	10	ns
End Write to Output Low-Z (KM64259B)	t_{OW}	0		0		0		ns
Data Valid to Output Valid (KM64260B)	t_{DO}				20		25	ns
Write to Output Valid (KM64260B)	t_{WO}				18		20	ns

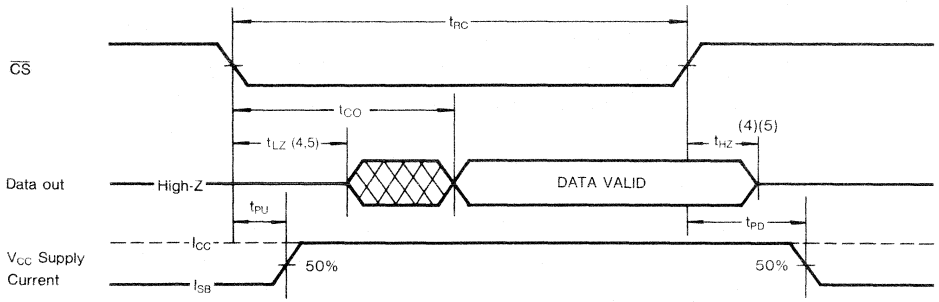
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH})



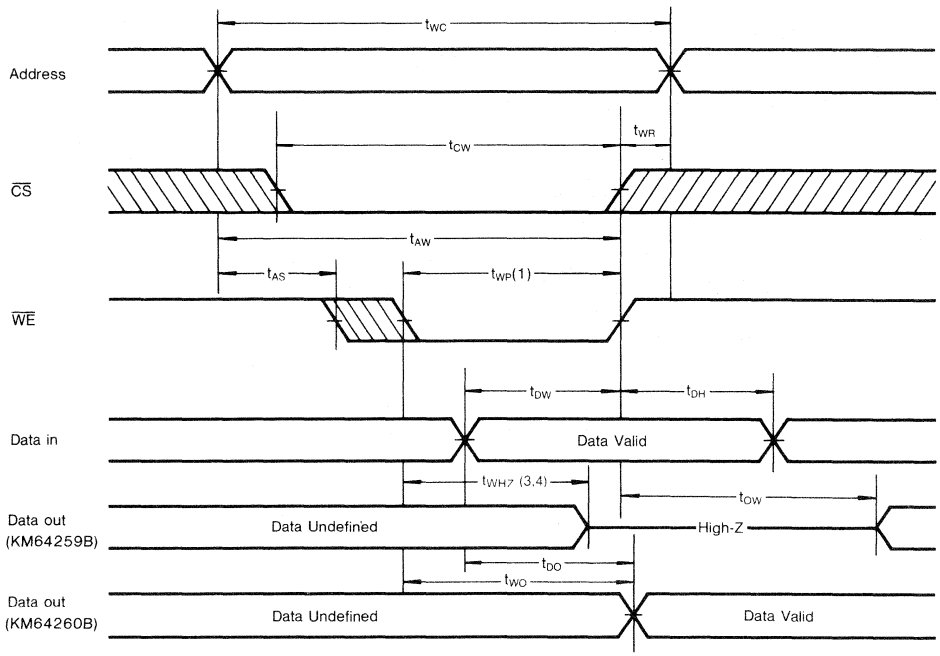
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



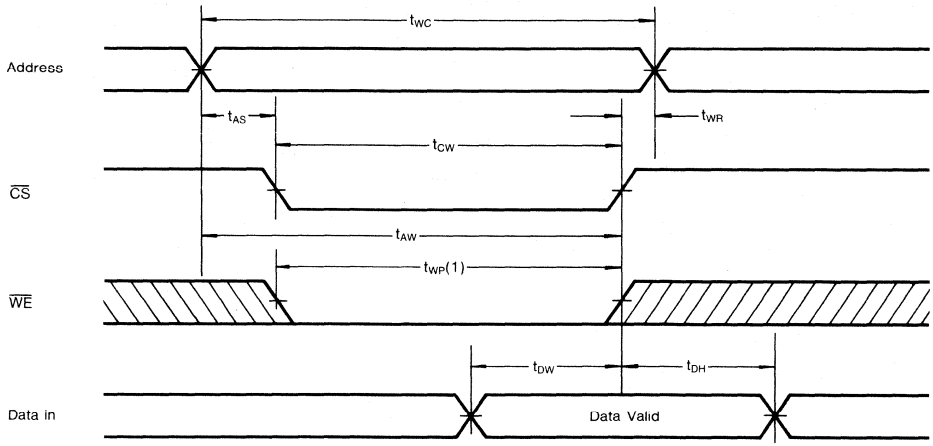
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (b).
5. This parameter is sampled and not 100% tested.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Note (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WHZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

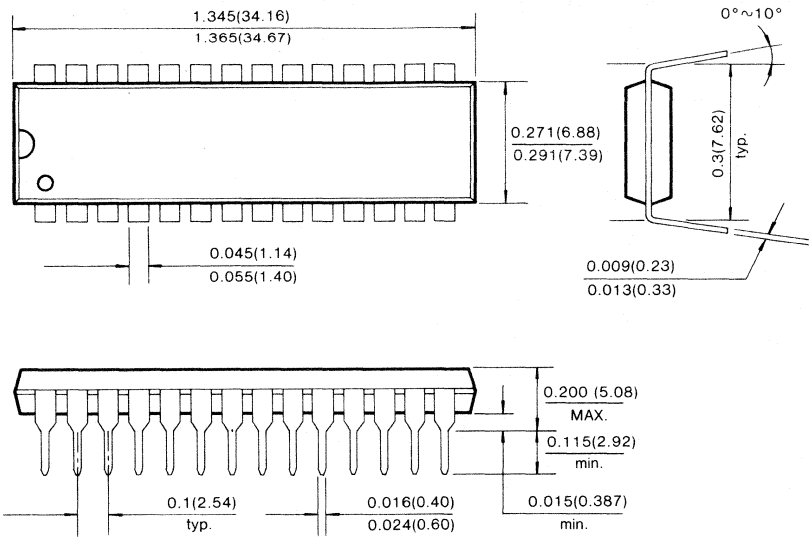
$\overline{CS}$	$\overline{WE}$	Mode	D_{OUT} Pin	Supply Current
H	X**	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	Read	D_{OUT}	I_{CC}
L	L	Write*	High-Z (KM64259B)	I_{CC}
			D_{OUT} (KM64260B)	

* Write cycle timing controlled by write enable ($\overline{WE}$)
** X means Don't Care

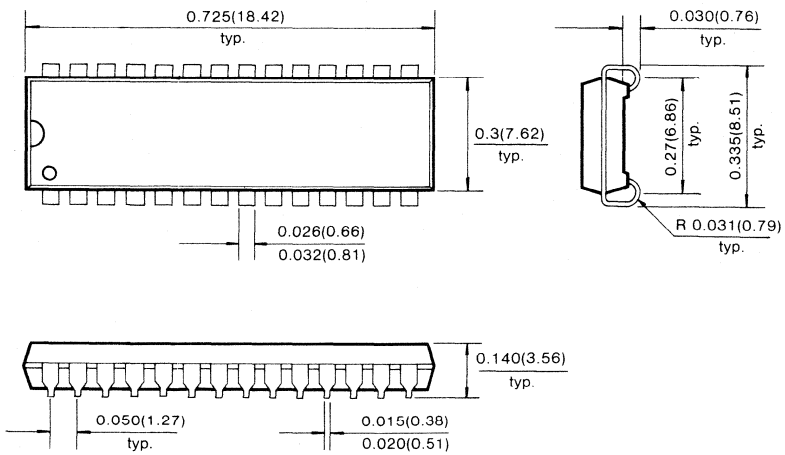
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



32KX8 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 20, 25ns (max)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS): 2mA (max)**
  - **Operating KM68257BP/J-15: 150mA (max.)**
  - **KM68257BP/J-20: 140mA (max.)**
  - **KM68257BP/J-25: 130mA (max.)**
- **Single 5V±10% Power Supply**
- **TTL Compatible inputs and outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM68257BP: 28-pin DIP (300 mil.)**
  - **KM68257BJ: 28-pin SOJ (300 mil.)**

GENERAL DESCRIPTION

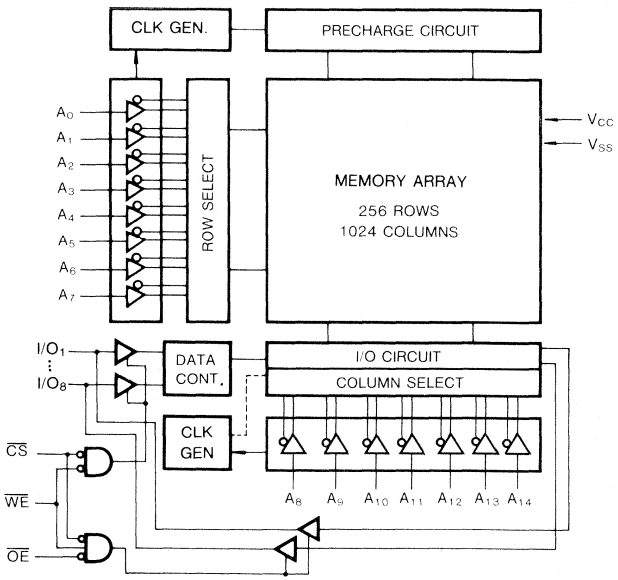
The KM68257B is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68257B uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology.

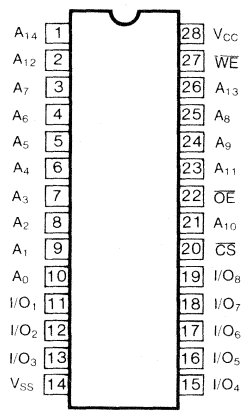
It is particularly well suited for use in high-density high-speed system applications.

The KM68257B is packaged in a 300 mil 28-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$I/O_1 \sim I/O_8$	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}				2	μA
Output Leakge Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}				2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	15ns			150	mA
			20ns			140	mA
			25ns			130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}				40	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}−0.2V, V_{IN}≥V_{CC}−0.2Vor V_{IN}≤0.2V				2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA				0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA		2.4			V

* Typ: V_{CC}=5V, T_A=25°C

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

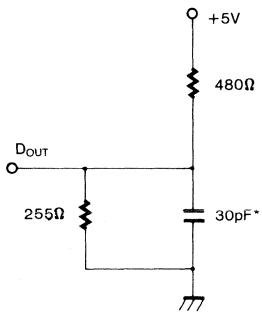
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

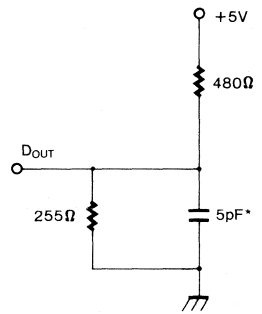
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68257BP-15 KM68257BJ-15		KM68257BP-20 KM68257BJ-20		KM68257BP-25 KM68257BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		15		20		25	ns

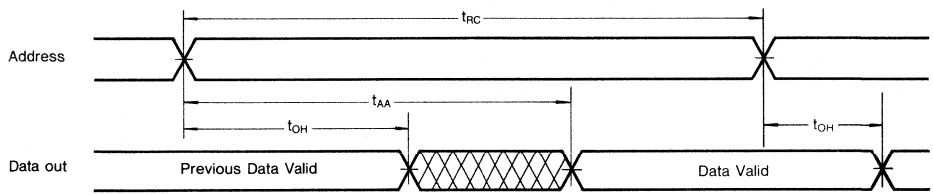
WRITE CYCLE

Parameter	Symbol	KM68257BP-15 KM68257BJ-15		KM68257BP-20 KM68257BJ-20		KM68257BP-25 KM68257BJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	9		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

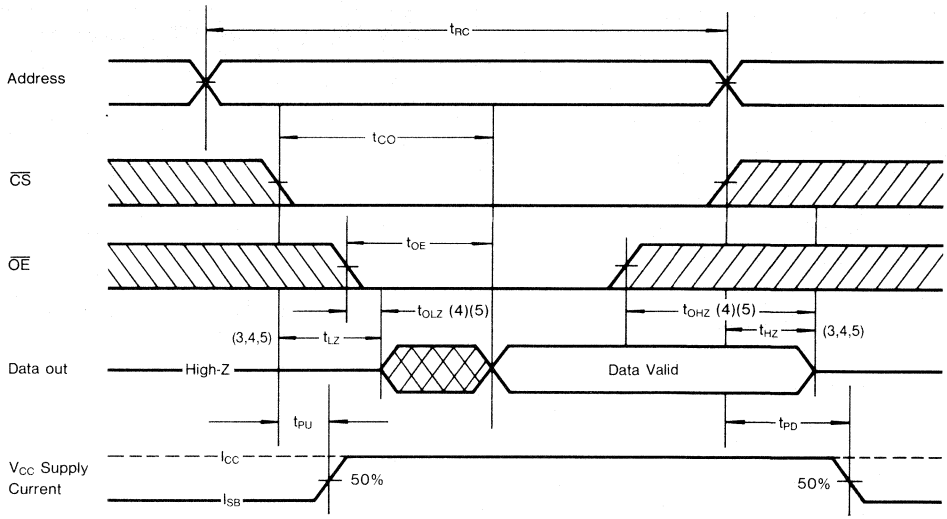
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



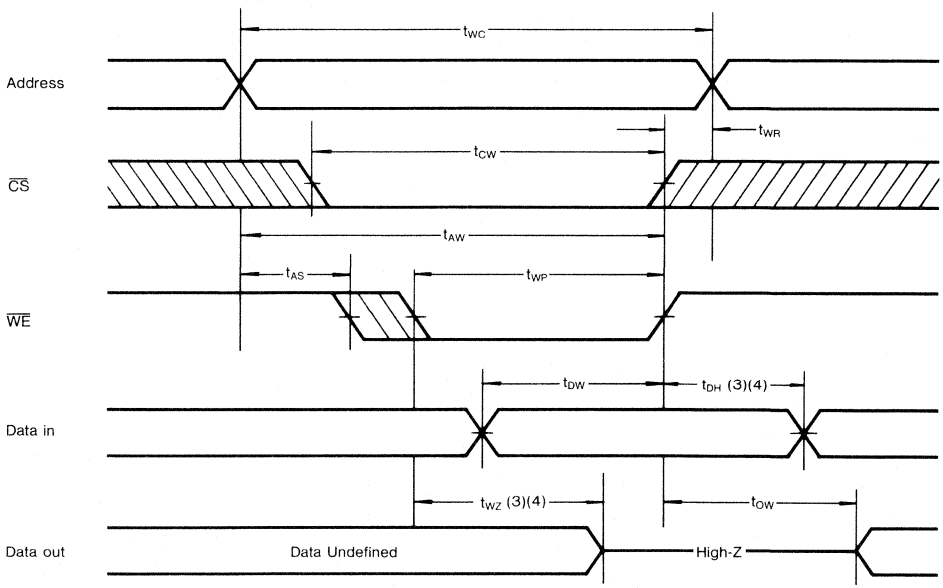
TIMING WAVEFORM OF READ CYCLE



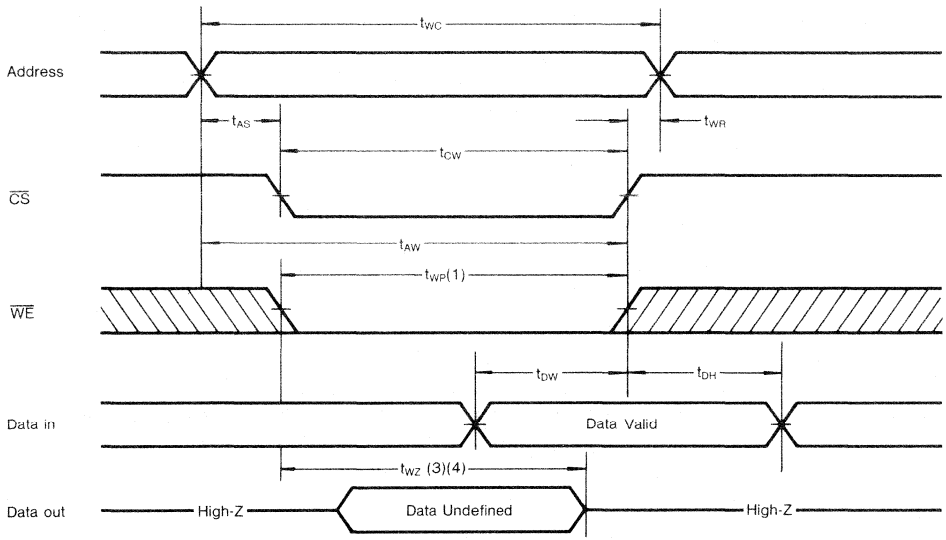
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

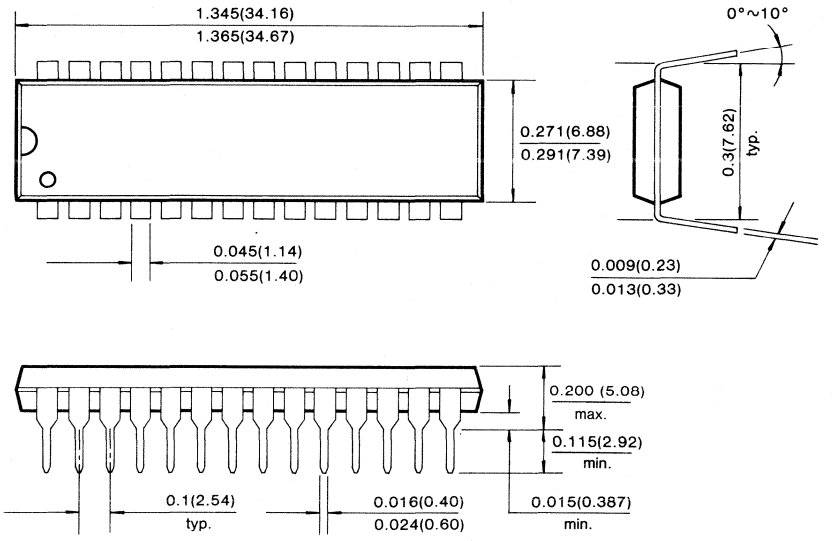
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X *	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care

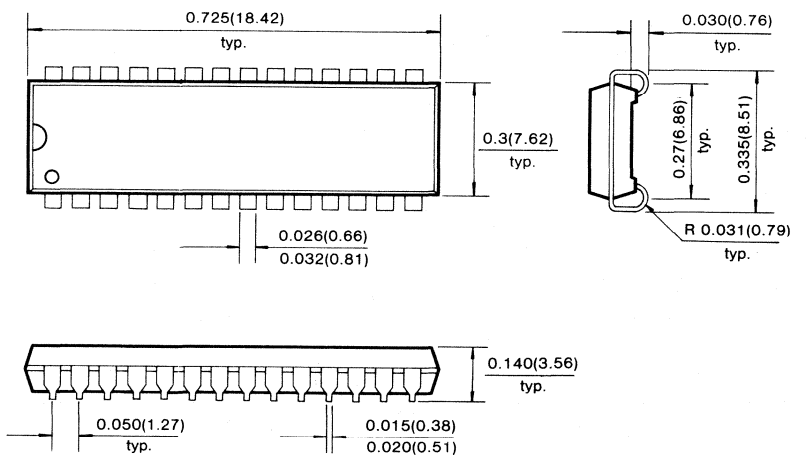
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE



32,768 WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 30mA (max.)**
  - **(CMOS): 100μA (max.)**
  - **Operating KM68257BLP/J-15: 150mA (max.)**
  - **KM68257BLP/J-20: 140mA (max.)**
  - **KM68257BLP/J-25: 130mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Low Data Retention Voltage: 2V (min.)**
- **Standard Pin Configuration**
  - **KM68257BLP: 28-pin DIP (300 mil)**
  - **KM68257BLJ: 28-pin SOJ (300 mil)**

GENERAL DESCRIPTION

The KM68257BL is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

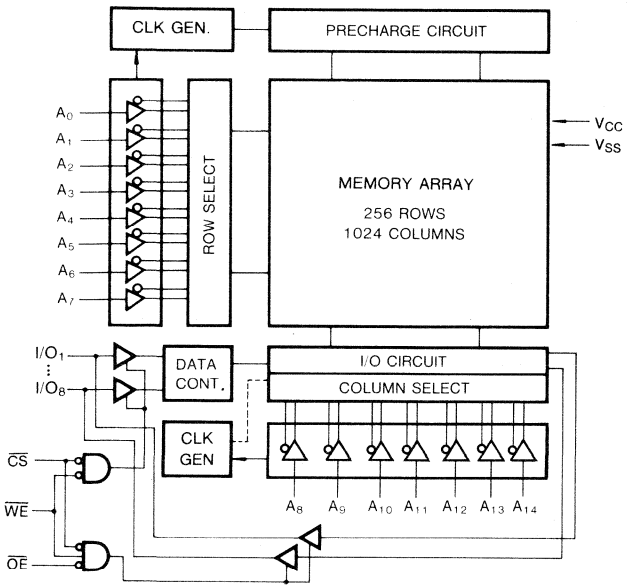
The KM68257BL uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications.

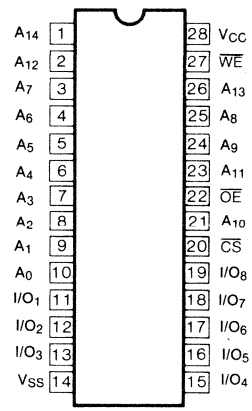
The KM68257BL is packaged in a 300 mil 28-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10 sec (Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}		—	—	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	15ns	—	—	150	mA
			20ns	—	—	140	mA
			25ns	—	—	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$		—	15	40	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$		—	2	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

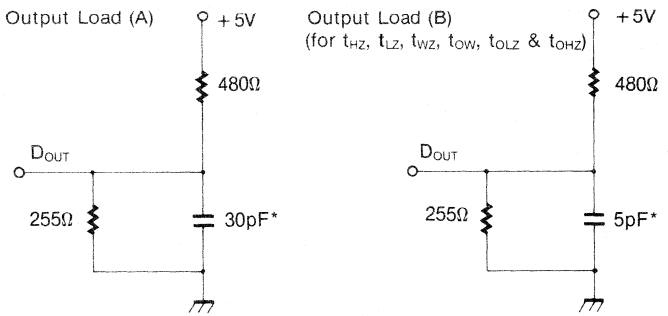
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68257BLP-15 KM68257BLJ-15		KM68257BLP-20 KM68257BLJ-20		KM68257BLP-25 KM68257BLJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Chip Select to Output	t_{CO}		15		20		25	ns
Output Enable to Valid Output	t_{OE}		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		15		20		25	ns

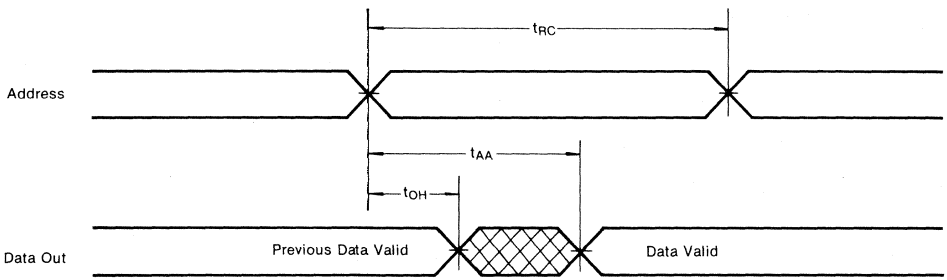
WRITE CYCLE

Parameter	Symbol	KM68257BLP-15 KM68257BLJ-15		KM68257BLP-20 KM68257BLJ-20		KM68257BLP-25 KM68257BLJ-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	8	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	9		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

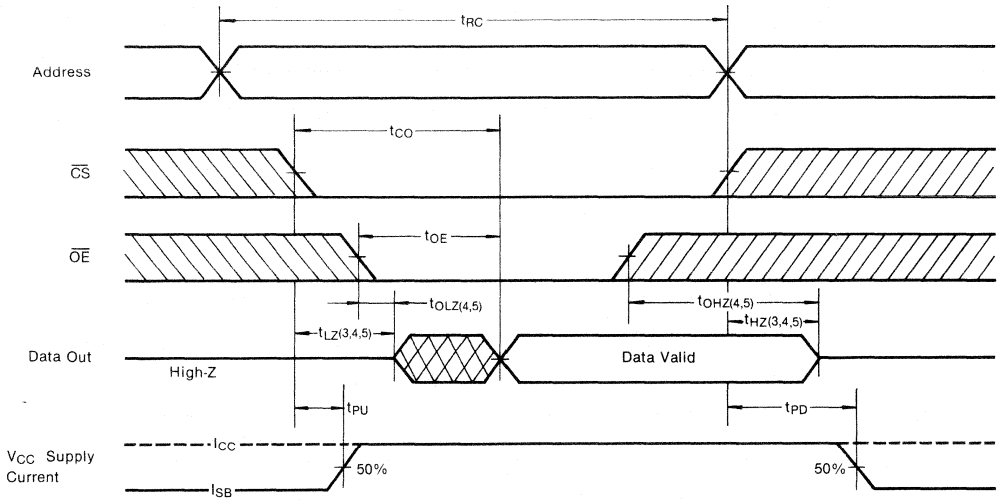
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



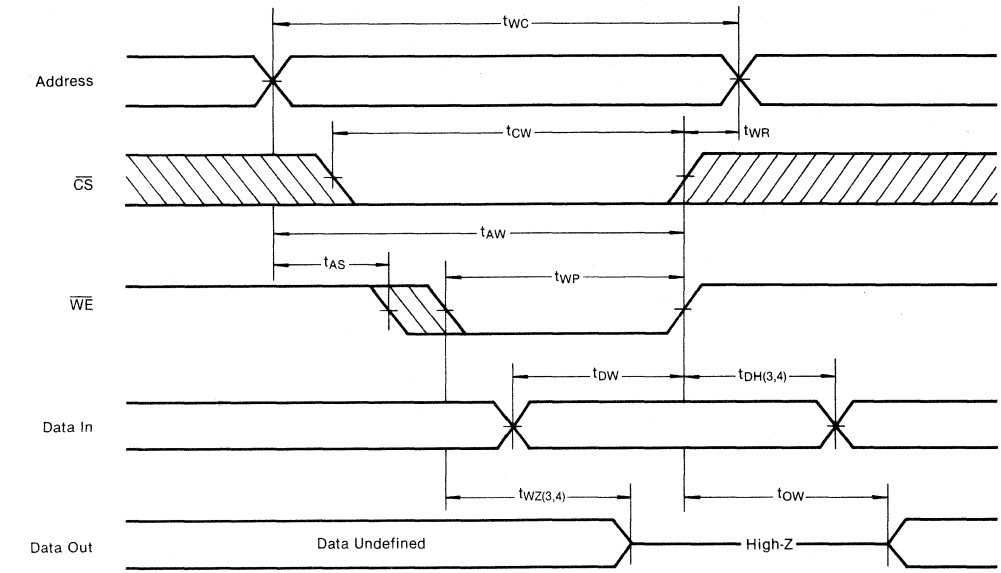
TIMING WAVEFORM OF READ CYCLE



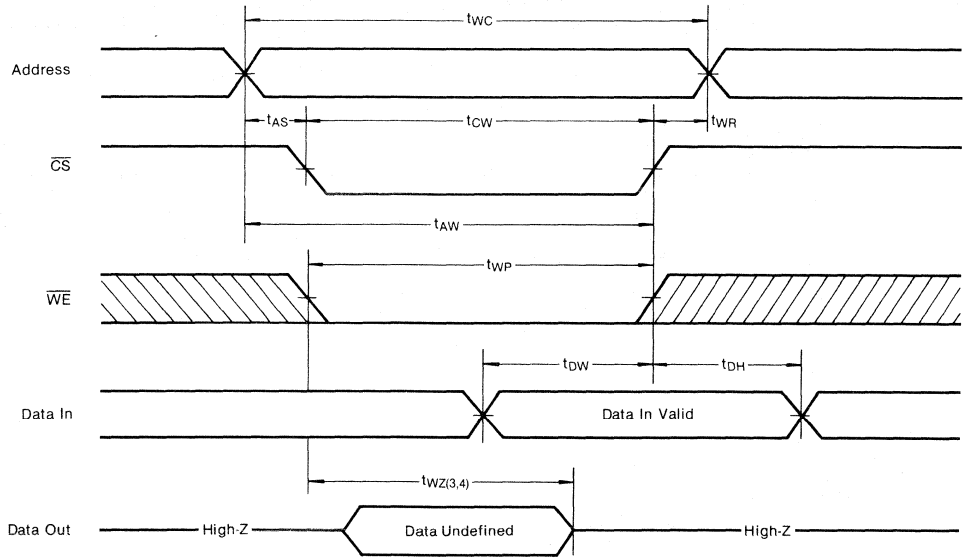
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

Notes

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

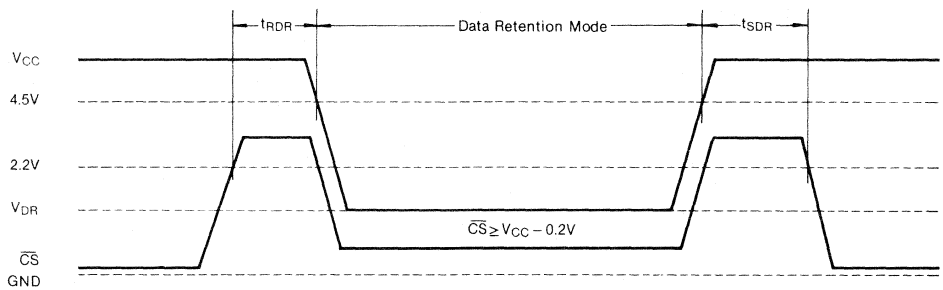
DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2		5.5	V
Data Retention Current	I_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$,		1	50*	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}**			ns

*: V_{CC} = 3V
**: t_{RC} = Read Cycle Time

2

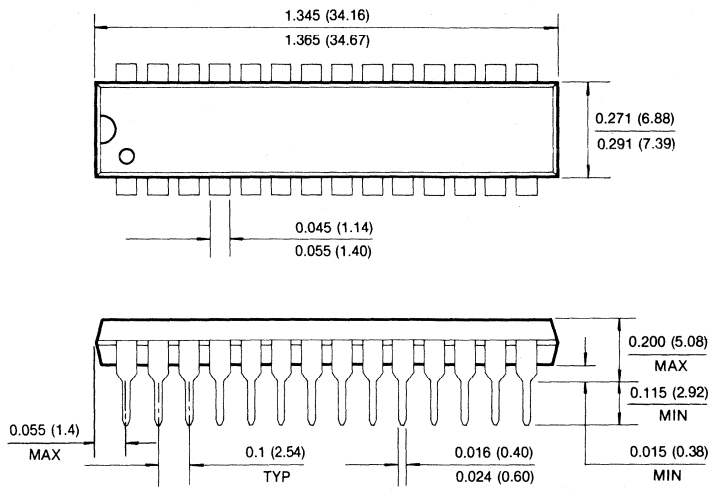
DATA RETENTION WAVEFORM



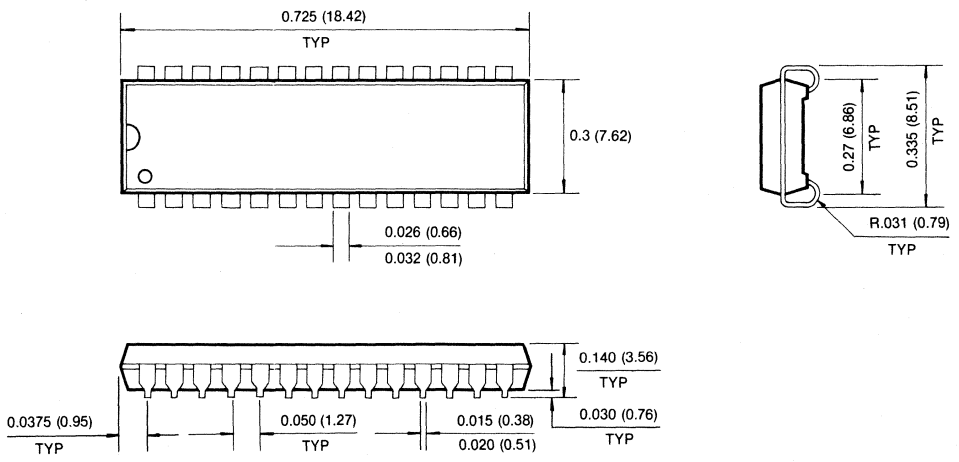
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



28 PIN SMALL OUT LINE J FORM PACKAGE



32,768 WORD×8 Bit High Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 10, 12ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 90mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM68B257AJ-8: 185mA (max.)**
  - **KM68B257AJ-10: 175mA (max.)**
  - **KM68B257AJ-12: 165mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM68B257AJ: 28-pin SOJ (300 mil)**

GENERAL DESCRIPTION

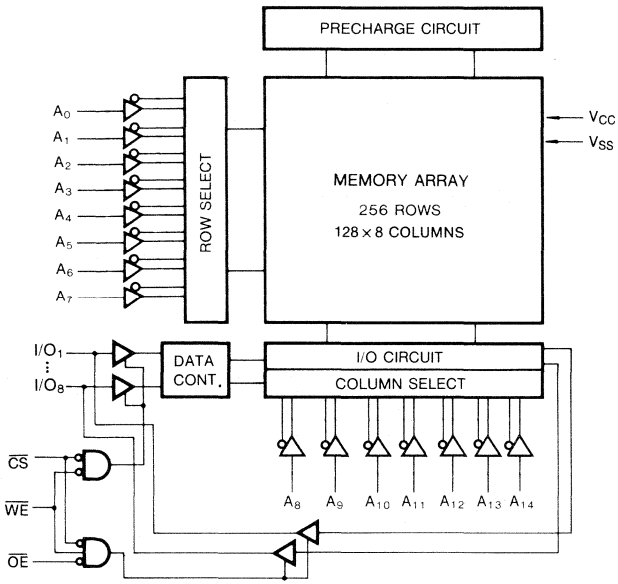
The KM68B257A is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68B257A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology.

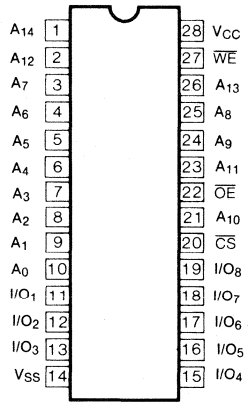
It is particularly well suited for use in high-density high-speed system applications.

The KM68B257A is packaged in a 300 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −2.0V ac (pulse width ≤ 8ns) for I ≤ 20mA
** V_{IH} (max.) = V_{CC} + 2V ac (pulse width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = V_{SS}$ to V_{CC}		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	8ns	—	185	mA
			10ns	—	175	mA
			12ns	—	165	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}/V_{IL}$, Min. Cycle		—	90	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2$ or $V_{IN} \leq 0.2V$		—	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note: Capacitance is sampled and not 100% tested.

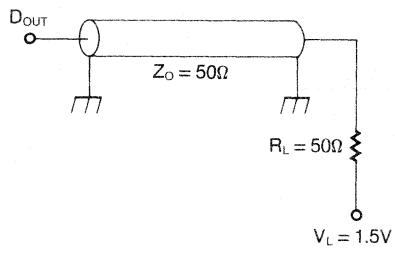
AC CHARACTERISTICS

TEST CONDITIONS

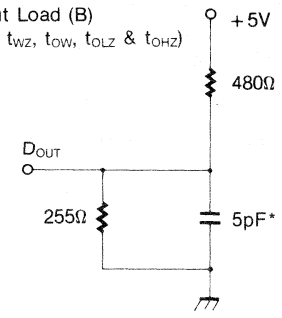
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

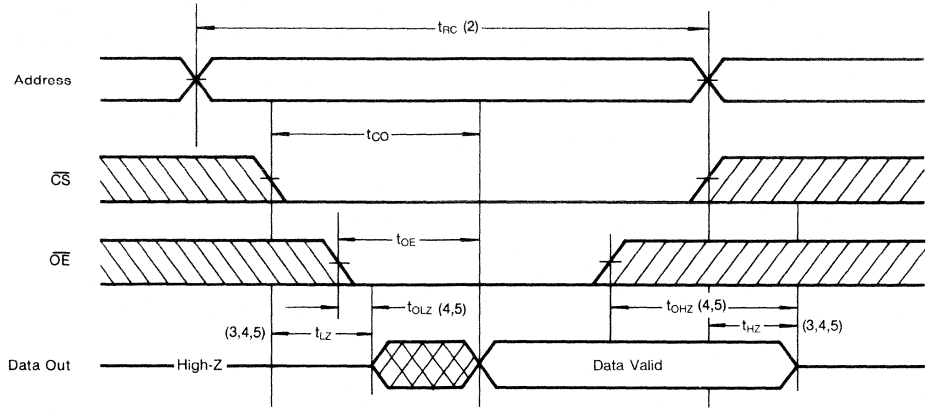
Parameter	Symbol	KM68B257A-8		KM68B257A-10		KM68B257A-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8		10		12		ns
Address Access Time	t_{AA}		8		10		12	ns
Chip Select to Output	t_{CO}		8		10		12	ns
Output Enable to Valid Output	t_{OE}		4		5		7	ns
Chip Enable to Low-Z Output	t_{LZ}	4		4		4		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	4		4		4		ns

WRITE CYCLE

Parameter	Symbol	KM68B257A-8		KM68B257A-10		KM68B257A-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8		10		12		ns
Chip Select to End of Write	t_{CW}	6		7		9		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	8		9		10		ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6		7		9		ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8		10		12		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4		5		6		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	4		4		4		ns

TIMING DIAGRAMS

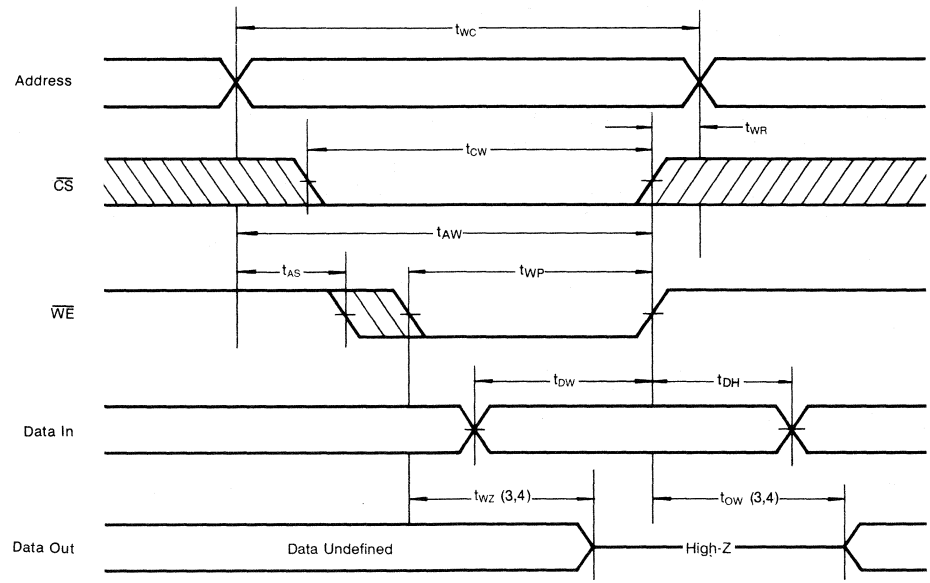
TIMING WAVEFORM OF READ CYCLE



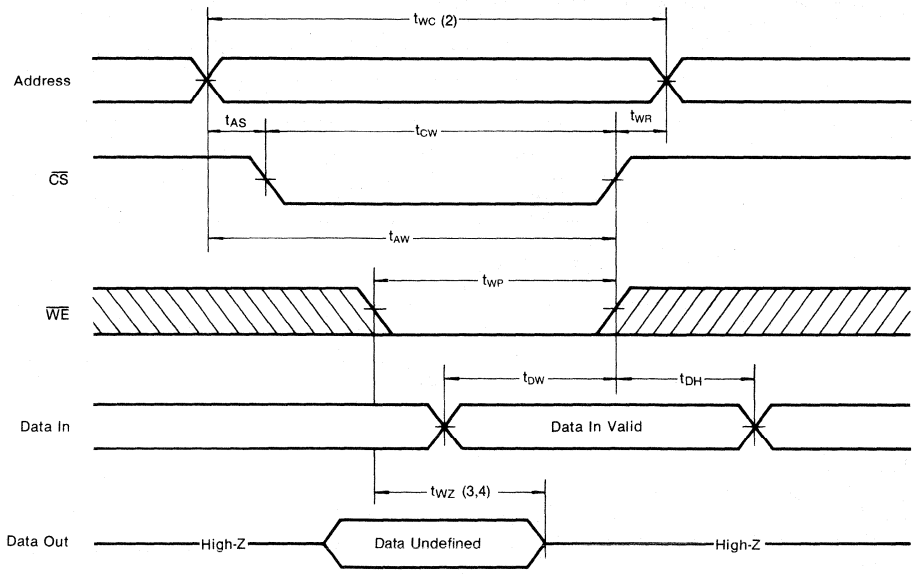
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
   This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.

FUNCTIONAL DESCRIPTION

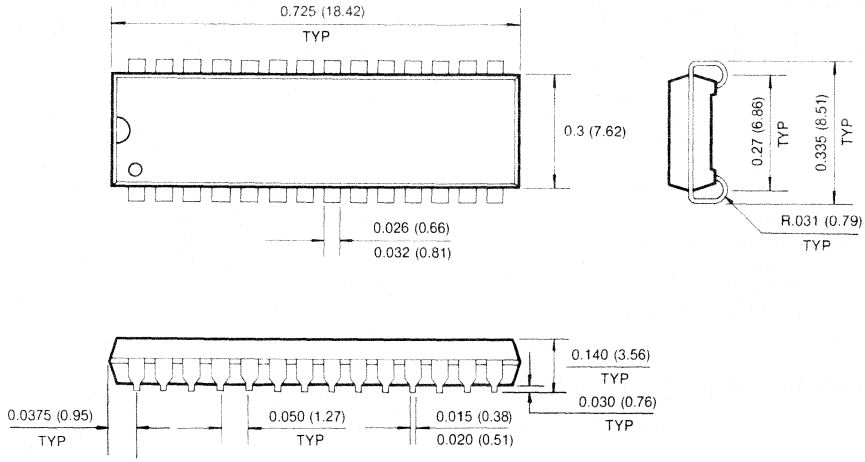
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

PACKAGE DIMENSIONS

Unit: Inches (millimeters)

28 PIN SMALL OUT LINE J FORM PACKAGE



32,768 WORD × 9 Bit High Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 10, 12ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 90mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM69B257AJ-8: 185mA (max.)**
  - **KM69B257AJ-10: 175mA (max.)**
  - **KM69B257AJ-12: 165mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM69B257AJ: 32-pin SOJ (300 mil)**

GENERAL DESCRIPTION

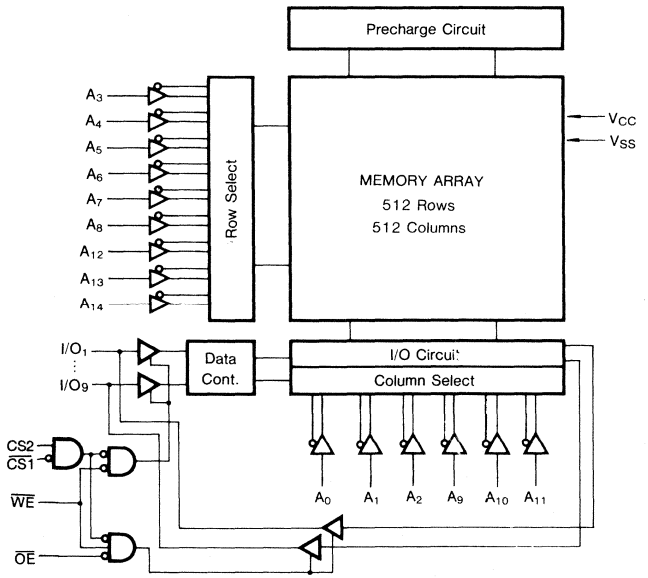
The KM69B257A is a 294,912-bit ultra high-speed Static Random Access Memory organized as 32,768 words by 9 bits. The device is manufactures using Samsung's advanced BiCMOS process.

The KM69B257A has an output enable pin which operates faster than address access time at read cycle.

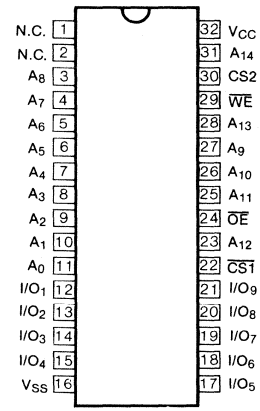
The KM69B257A has been designed for high speed applications. It is particulary well suited for applications requiring high speed, local instruction cache large byte wide cache, or very fast data buffering in personal computers, workstations, and communications. The parity (9th) bit markes the KM69B257A ideal for OLTP system, and i486 based system.

The KM69B257A is packaged in a 300 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS_1}$, CS_2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_9	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −2.0V ac (pulse width ≤ 8ns) for I ≤ 20mA
** V_{IH} (max.) = V_{CC} +2V ac (pulse width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL}, V_{OUT} = V_{SS} to V_{CC}		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS1}$ = V_{IL}, CS2 = V_{IH} I_{OUT} = 0mA	8ns	—	185	mA
			10ns	—	175	mA
			12ns	—	165	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} V_{IN} = V_{IH}/V_{IL}, Min. Cycle		—	90	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{CC} − 0.2V or CS2 ≤ 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} − 0.2V		—	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note: Capacitance is sampled and not 100% tested.

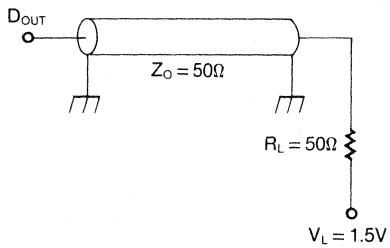
AC CHARACTERISTICS

TEST CONDITIONS

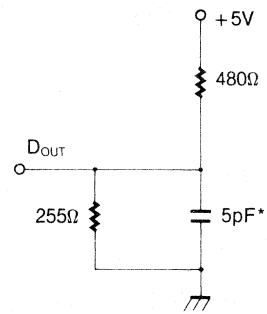
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



READ CYCLE

Parameter	Symbol	KM69B257A-8		KM69B257A-10		KM69B257A-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8		10		12		ns
Address Access Time	t_{AA}		8		10		12	ns
Chip Select to Output	$t_{CO1, CO2}$		8		10		12	ns
Output Enable to Valid Output	t_{OE}		4		5		7	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	4		4		4		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	4		4		4		ns

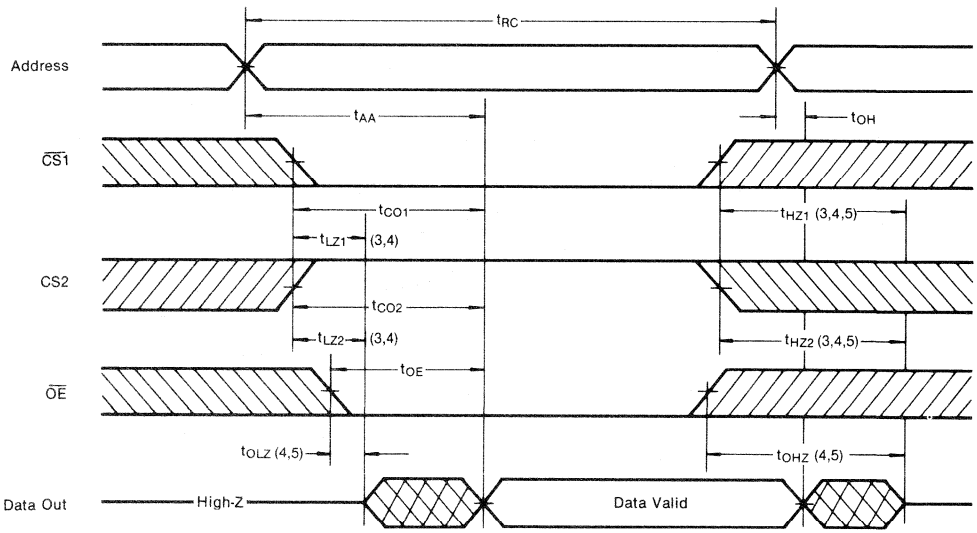
WRITE CYCLE

Parameter	Symbol	KM69B257A-8		KM69B257A-10		KM69B257A-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8		10		12		ns
Chip Select to End of Write	t_{CW}	6		7		9		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	8		9		10		ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	6		7		9		ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8		10		12		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4		5		6		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	4		4		4		ns

2

TIMING DIAGRAMS

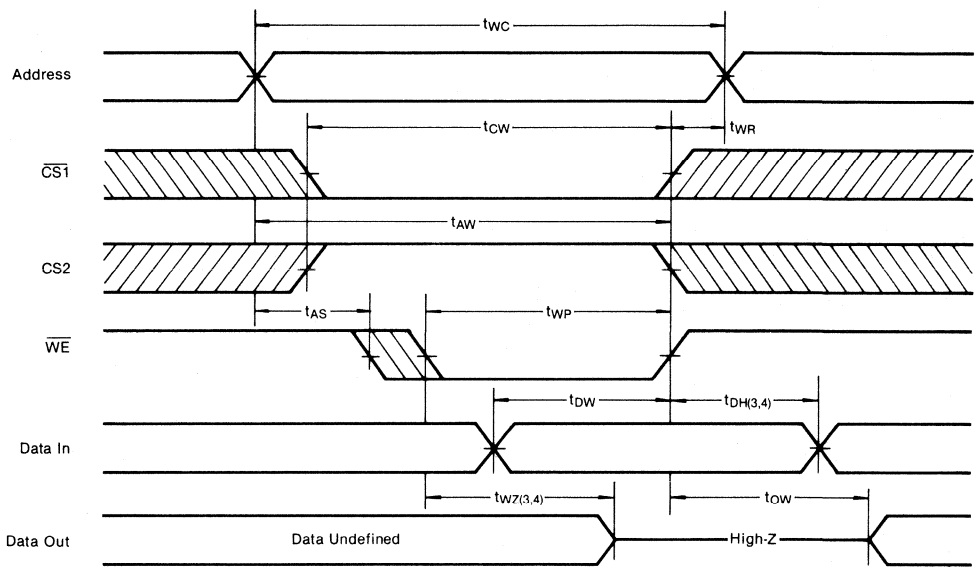
TIMING WAVEFORM OF READ CYCLE



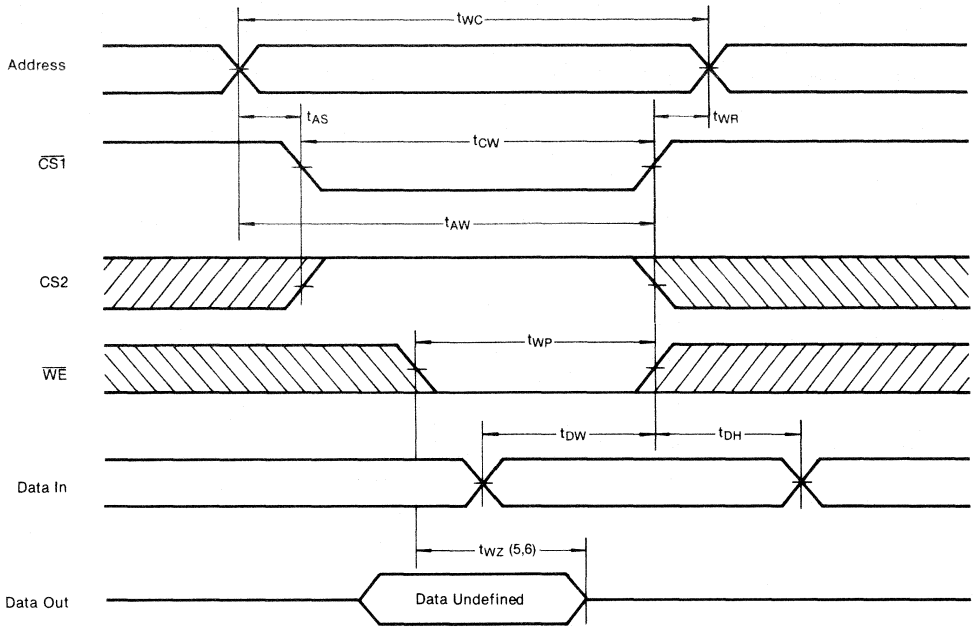
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

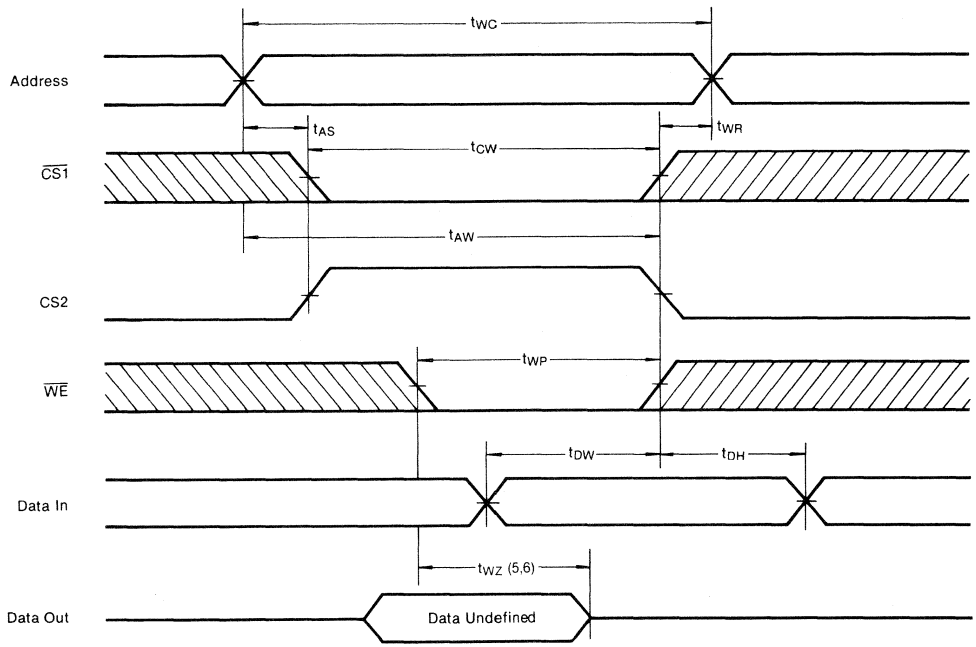
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and WE going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{CS1}$,CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

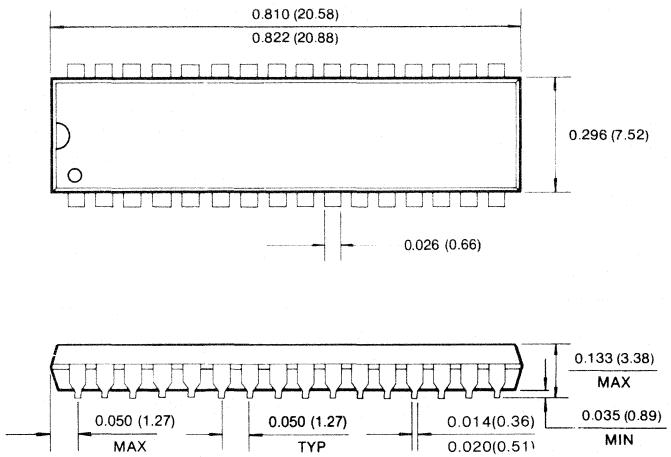
FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

PACKAGE DIMENSIONS

32 PIN SMALL OUT LINE J FORM PACKAGE



32,768 WORD × 16 BIT High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time 17, 20, 25ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS): 2mA (max.)**
  - **Operating KM616513J-17: 180mA (max.)**
  - **KM616513J-20: 160mA (max.)**
  - **KM616513J-25: 140mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Data Byte Control ($\overline{LB}$: $I/O_1 \sim I/O_8$, $\overline{UB}$: $I/O_9 \sim I/O_{16}$)**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Output**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  - **KM616513J: 40-Pin SOJ (400 mil.)**

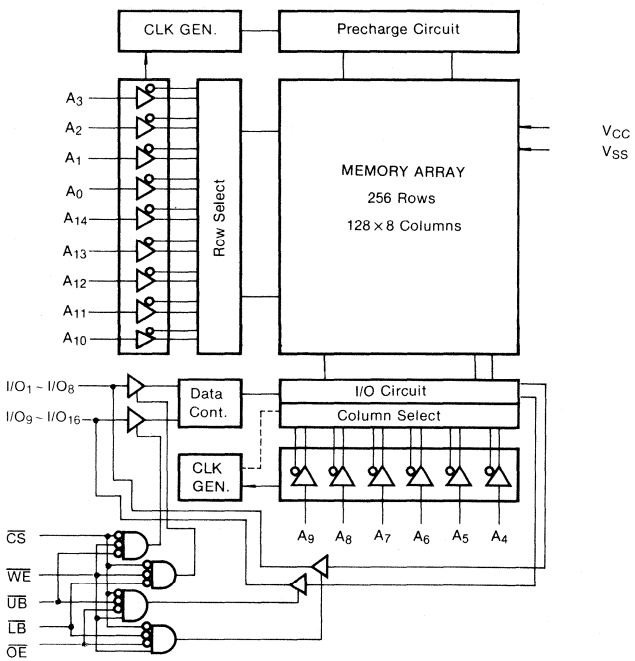
GENERAL DESCRIPTION

The KM616513 is a 524,288-bit high speed static random access memory organized as 32,768 words by 16 bits.

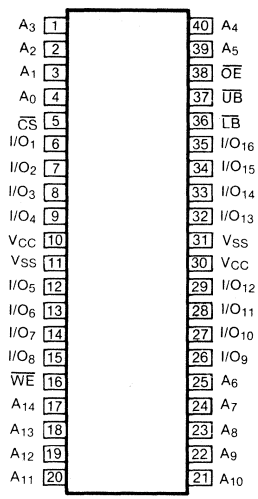
The KM616513 uses sixteen common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM616513 is packaged in a 400 mil. 40-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
I/O_1-I/O_{16}	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −3.0V for ≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = V_{SS}$ to V_{CC}		—	10	μA
Average Operating Current	I_{CC1}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	17ns	—	180	mA
			20ns	—	160	mA
			25ns	—	140	mA
			100ns	—	80	mA
	I_{CC2}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA $\overline{UB} = V_{IL}$, $\overline{LB} = V_{IH}$ or $\overline{UB} = V_{IH}$, $\overline{LB} = V_{IL}$	17ns	—	130	mA
			20ns	—	110	mA
			25ns	—	100	mA
			100ns	—	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}/V_{IL}$, Min. Cycle		—	40	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		—	2	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA		2.4	—	V

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

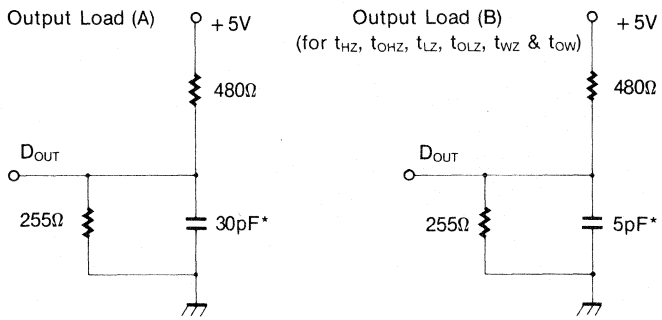
Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS

($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616513-17		KM616513-20		KM616513-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		ns
Address Access Time	t_{AA}		17		20		25	ns
Chip Select to Output	t_{CO}		17		20		25	ns
Output Enable to Valid Output	t_{OE}		9		10		13	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}		17		20		25	ns
Output Enable to Low-Z Output	t_{OLZ}	2		3		3		ns
Chip Enable to Low-Z Output	t_{LZ}	5		5		5		ns
$\overline{LB}$, $\overline{UB}$ Enable to Low-Z Output	t_{BLZ}	5		5		5		ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	8	ns
Chip Disable to High-Z Output	t_{HZ}	0	8	0	9	0	9	ns
$\overline{LB}$, $\overline{UB}$ Disable to High-Z Output	t_{BHZ}	0	8	0	9	0	9	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns

WRITE CYCLE

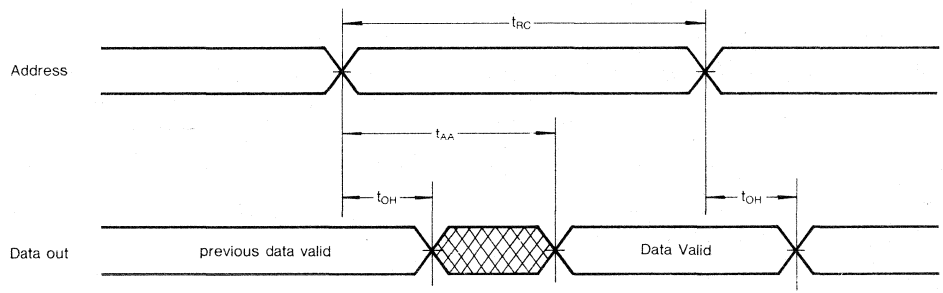
Parameter	Symbol	KM616513-17		KM616513-20		KM616513-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	12		13		15		ns
Write Pluse Width ($\overline{OE}$ Low)	t_{WP}	17		20		25		ns
LB, UB Valid to End of Write	t_{BW}	12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WZ}	0	9	0	10	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		5		ns

2

TIMING DIAGRAMS

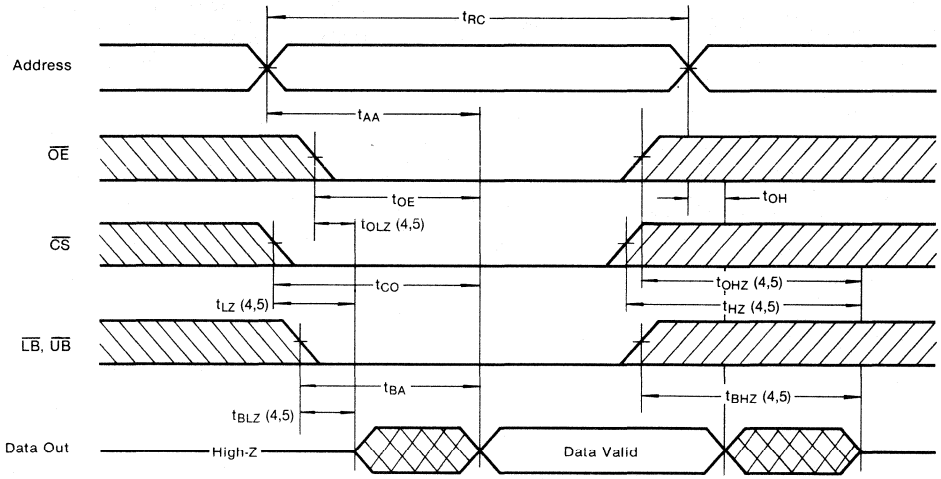
TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



TIMING DIAGRAMS

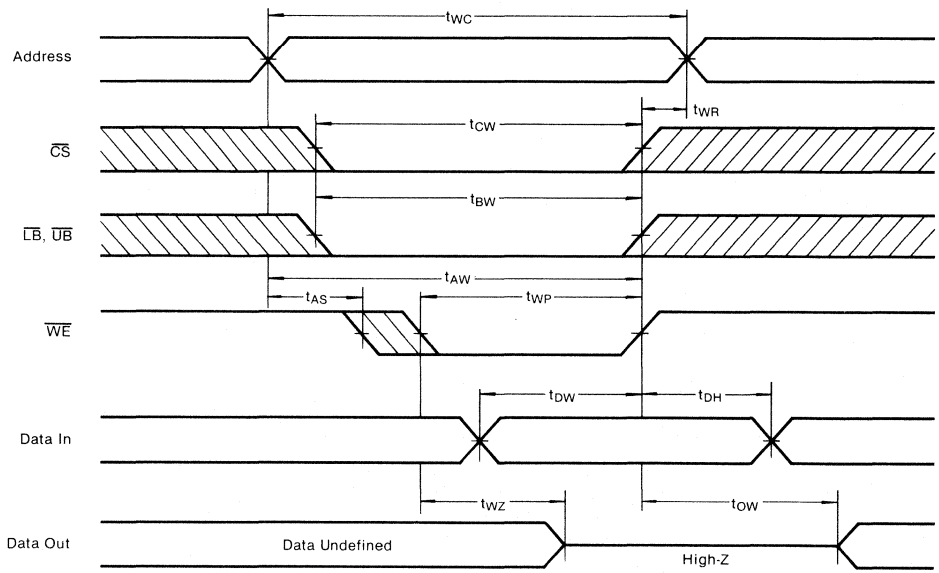
TIMING WAVEFORM OF READ CYCLE



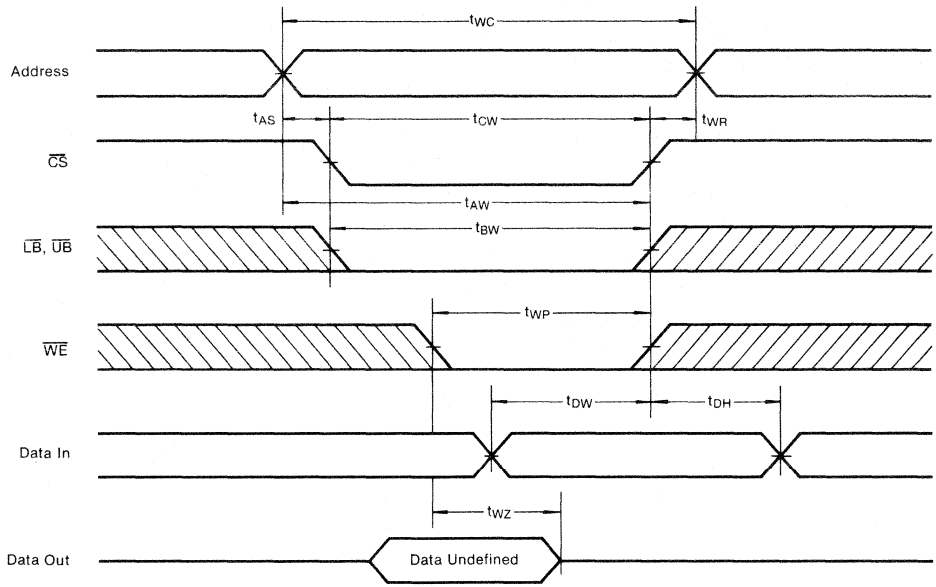
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.

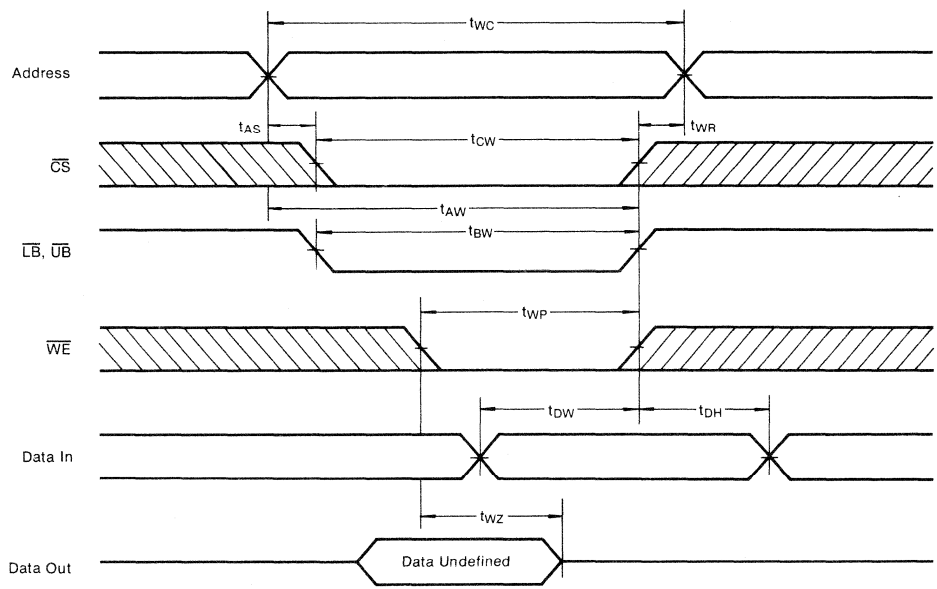
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
   A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low.
   A write end at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS}$ is low; I/O pins are in the output state.
   The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

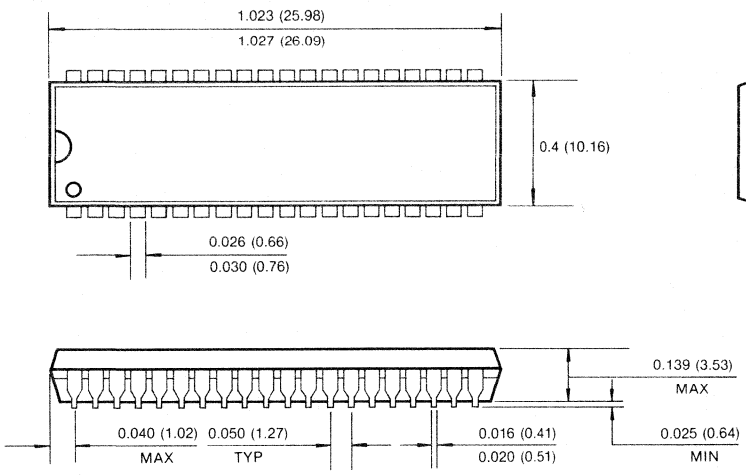
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						$I/O_1 \sim I/O_8$	$I/O_9 \sim I/O_{16}$	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* Note: X means Don't Care.

PACKAGE DIMENSIONS

40 LEAD PLASTIC SMALL OUT LINE J FORM PACKAGE

Unit: Inches (millimeters)



1MX1 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time 20,25,35ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA (max.)**
  - **Operating KM611001P/J-20: 130mA (max)**
  - **KM611001P/J-25: 110mA (max)**
  - **KM611001P/J-35: 100mA (max)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **-No clock or refresh required**
- **Three state Output**
- **Standard Pin Configuration**
  - **KM611001P: 28-pin DIP (400mil)**
  - **KM611001J: 28-pin SOJ (400mil)**

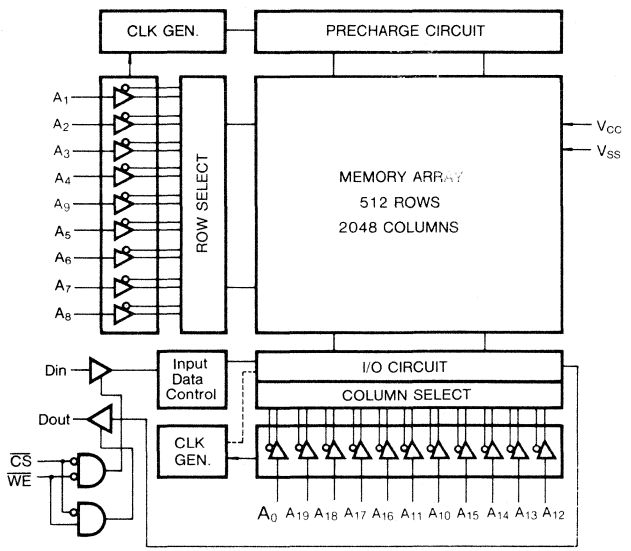
GENERAL DESCRIPTION

The KM611001 is a 1,048,576-bit high-speed static random access memory organized as 1,048,576 words by 1 bit.

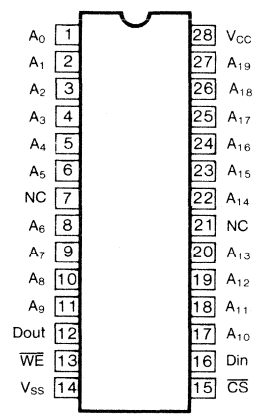
The KM611001 has separate input and output lines for fast read and write access. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high-speed system applications.

The KM611001 is packaged in a 400mil 28-pin plastic DIP or SOJ with the conventional power-supply pinout.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
Ao-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	20ns		130	mA
			25ns		110	mA
			35ns		100	mA
Standby Power Supply Current	I_{sb}	$\overline{CS}$=V_{IH}			40	mA
	I_{sb1}	$\overline{CS}$≥V_{CC}-0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA		2.4		V

*TYP: V_{CC}=5V, T_A=25°C.

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	7	pF

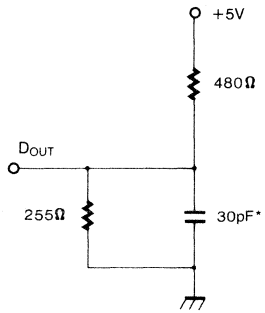
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

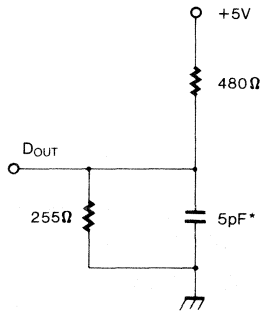
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM611001-20		KM611001-25		KM611001-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO}		20		25		35	ns
Chip Select to Low-Z Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		20		25		35	ns

WRITE CYCLE

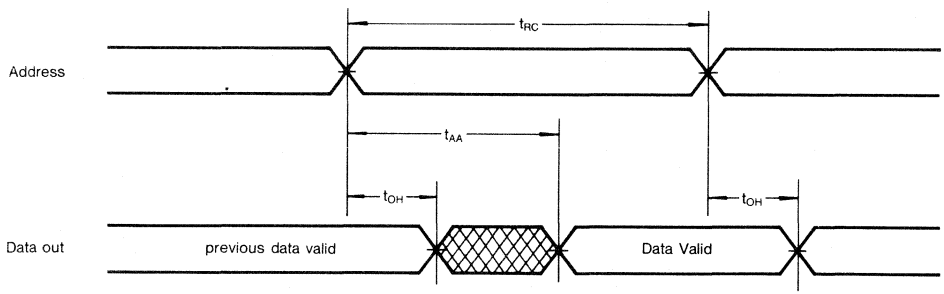
Parameter	Symbol	KM611001-20		KM611001-25		KM611001-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Write Pluse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

2

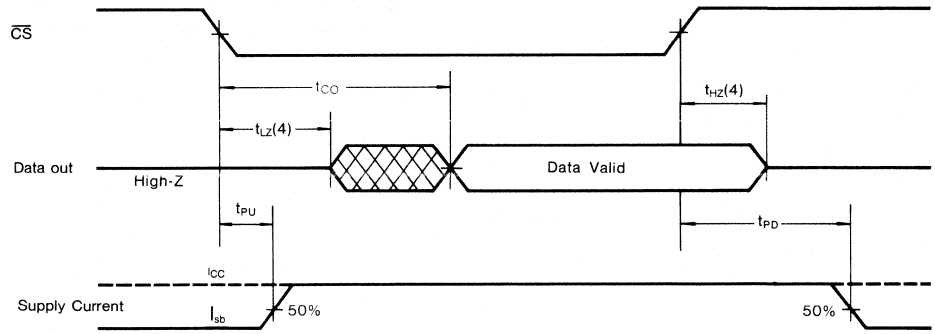
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH})



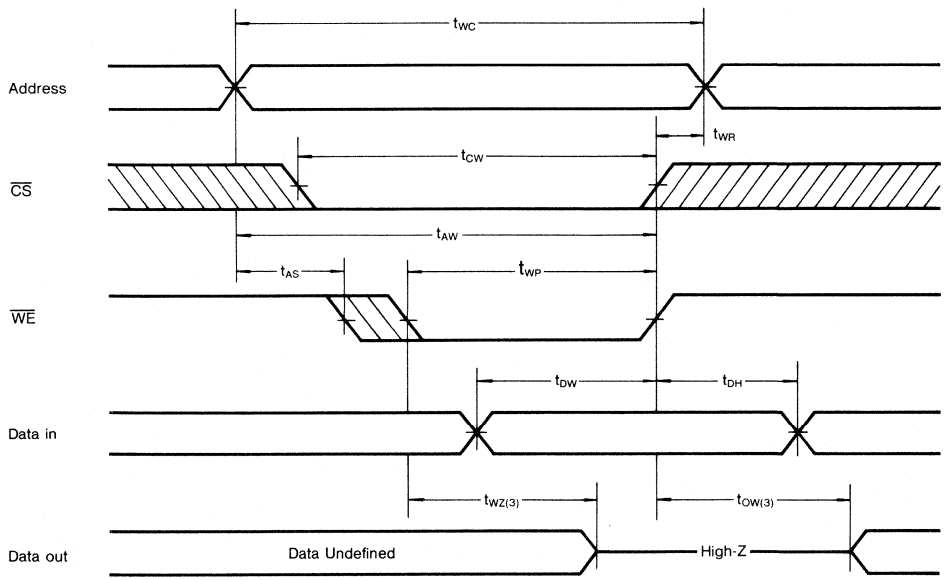
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



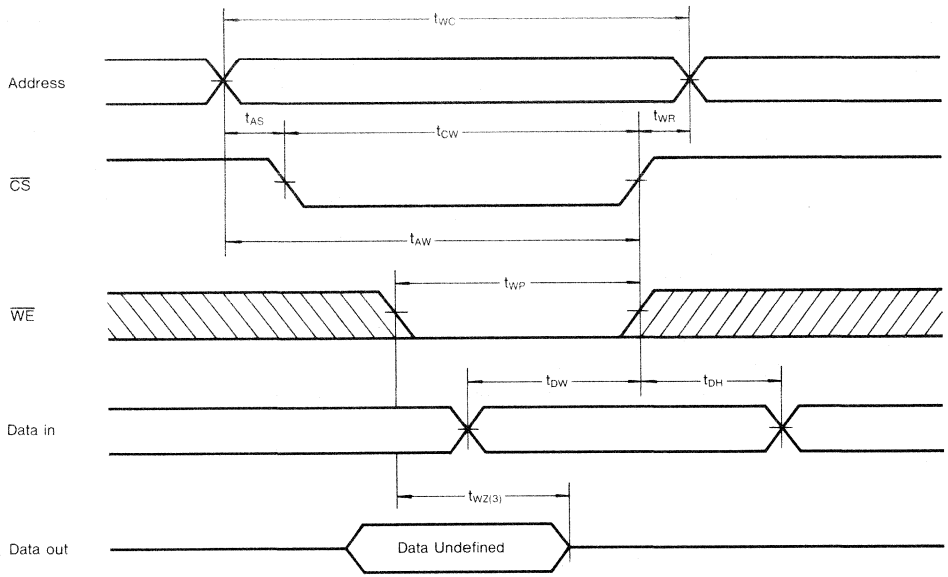
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

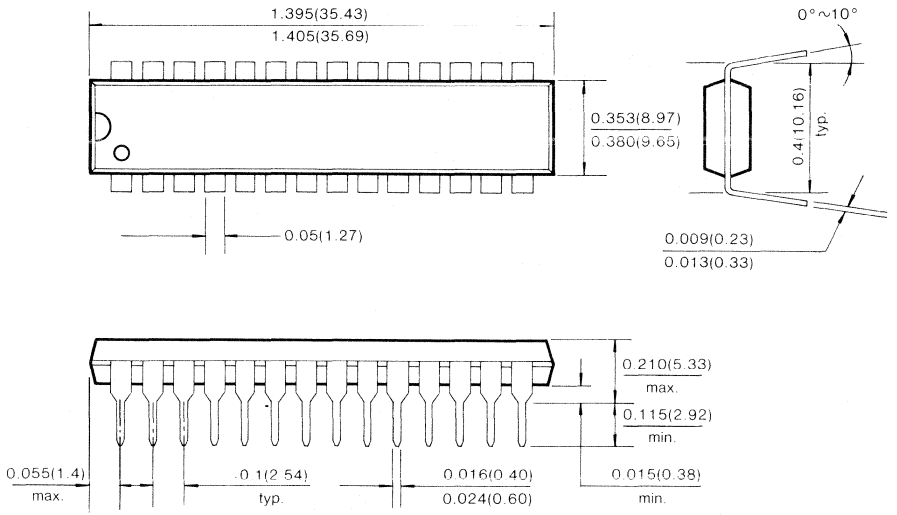
$\overline{CS}$	$\overline{WE}$	Dout PIN	Supply Current	Mode
H	X*	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	Dout	I_{CC}	Read
L	L	High-Z	I_{CC}	Write

*Note: X means Don't Care

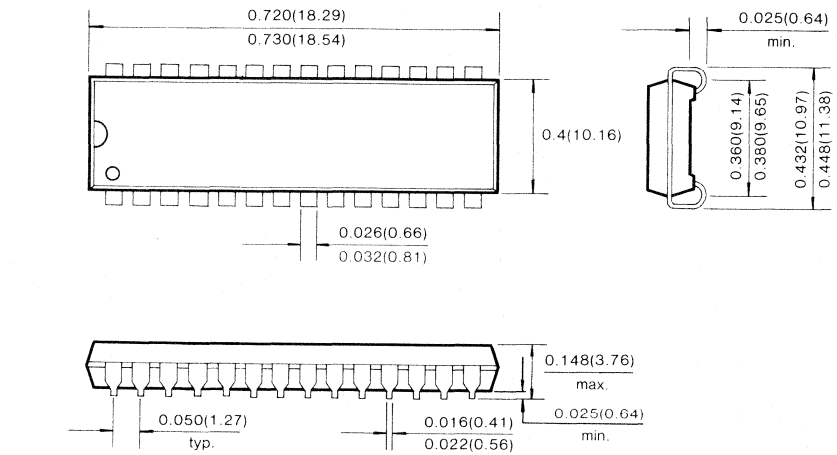
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE (400 mil)

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE (400 mil)



256KX4 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time 20,25,35ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA (max.)**
  - **Operating KM641001P/J-20: 150mA (max)**
  - **KM641001P/J-25: 130mA (max)**
  - **KM641001P/J-35: 110mA (max)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **-No clock or refresh required**
- **Three state Output**
- **Standard Pin Configuration**
  - **KM641001P: 28-pin DIP (400mil)**
  - **KM641001J: 28-pin SOJ (400mil)**

GENERAL DESCRIPTION

The KM641001 is a 1,048,576-bit high-speed static random access memory organized as 262,144 words by 4 bit.

The KM641001 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM641001 is packaged in a 400mil 28-pin plastic DIP or SOJ with the conventional power-supply pinout.

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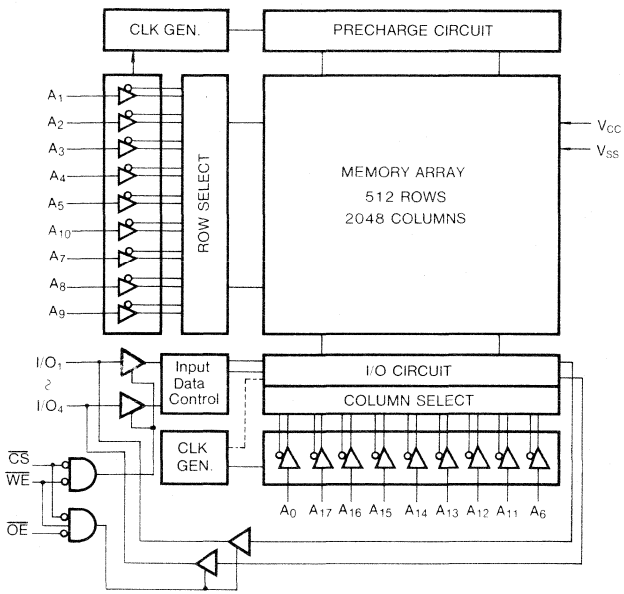
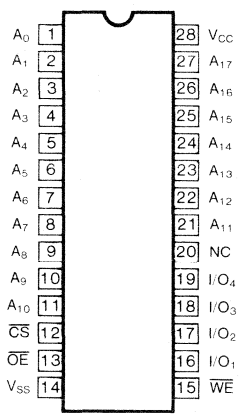
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Inputs/Outputs
VCC	Power (+5V)
VSS	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT}=V_{SS} to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	20ns		150	mA
			25ns		130	mA
			35ns		110	mA
Standby Power Supply Current	I_{sb}	$\overline{CS}$=V_{IH}			40	mA
	I_{sb1}	$\overline{CS}$≥V_{CC}-0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA		2.4		V

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

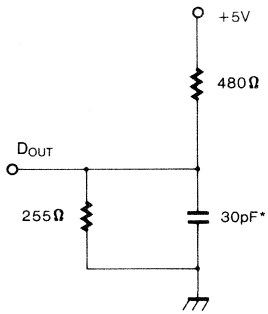
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

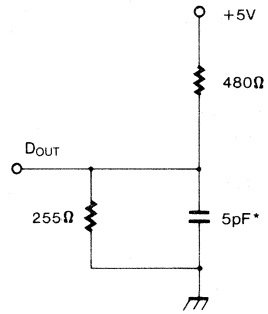
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641001-20		KM641001-25		KM641001-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{ACS}		20		25		35	ns
Output Enable to Output	t_{OE}		10		13		15	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ}	0		0		0		ns
Output Disable to Hgih-Z Output	t_{OHZ}	0	8	0	10		15	
Chip Disable to High-Z Output	t_{HZ}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns
Chip Select to Power Up Time	t_{PU}	0		0		0		ns
Chip Disable to Power Down Time	t_{PD}		20		25		35	ns

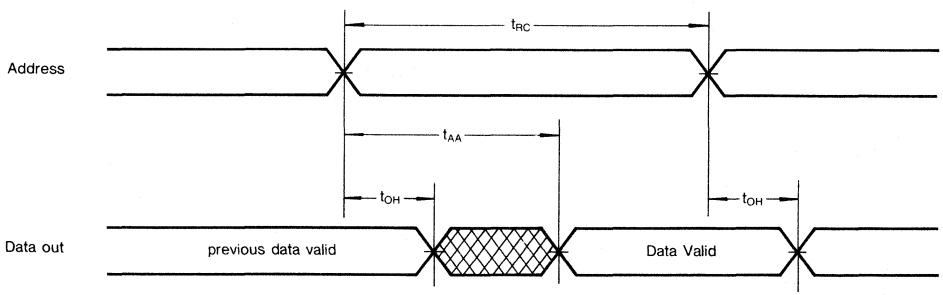
WRITE CYCLE

Parameter	Symbol	KM641001-20		KM641001-25		KM641001-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Write Pluse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

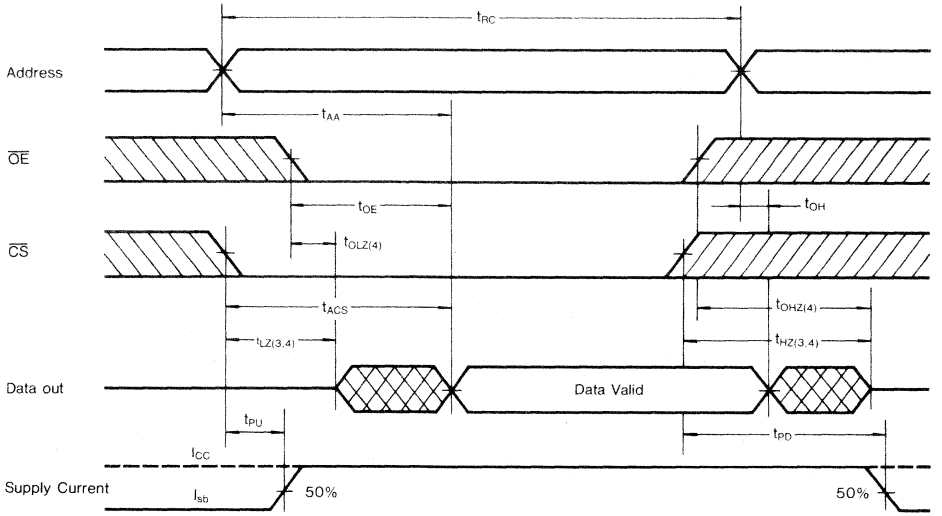
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



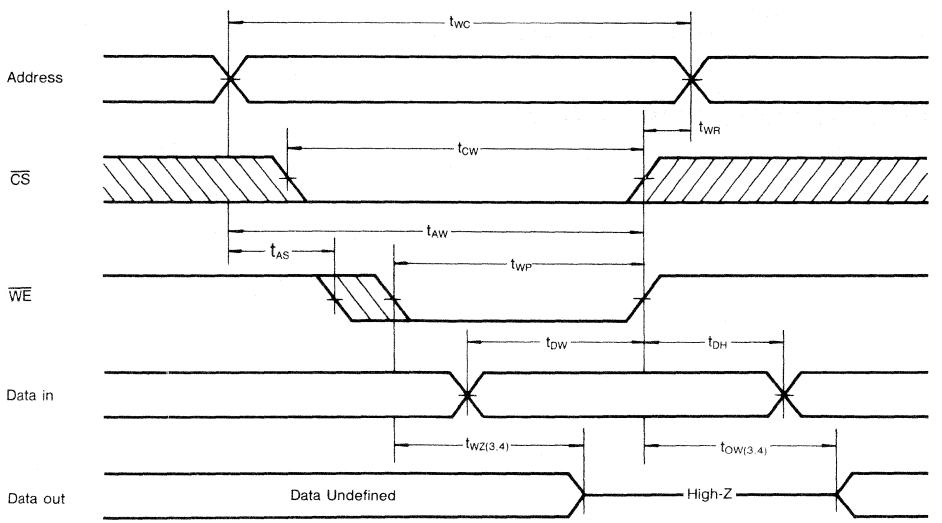
TIMING WAVEFORM OF READ CYCLE



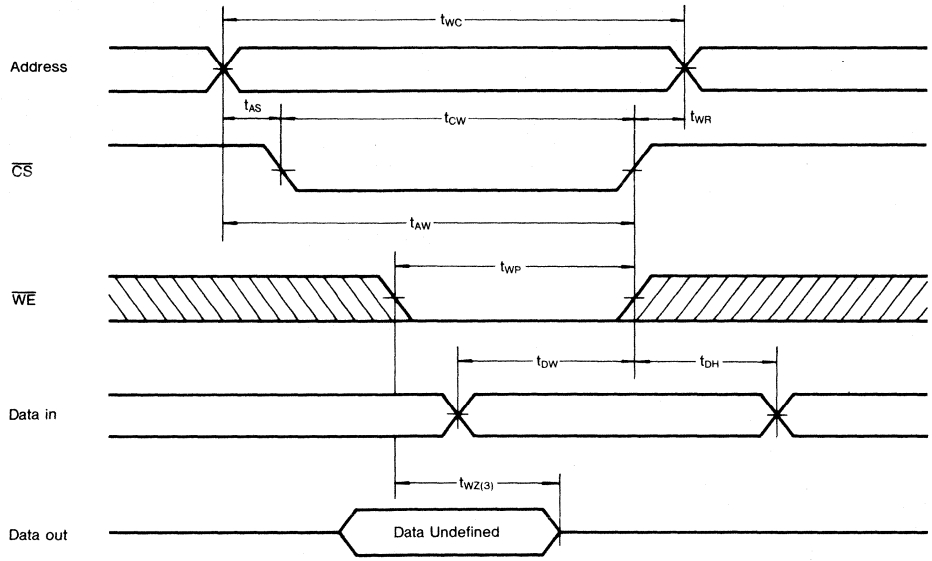
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

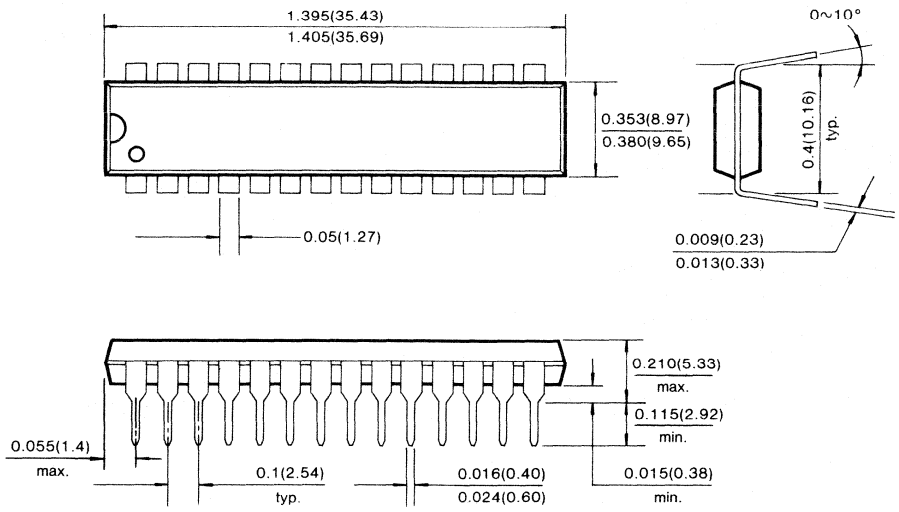
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O PIN	Supply Current	Mode
H	X	X*	High-Z	I_{sb}, I_{sb1}	Not Select
L	L	H	Dout	I_{CC}	Read
L	L	L	Din	I_{CC}	Write
L	H	L	Din	I_{CC}	Write

*Note: X means Don't Care

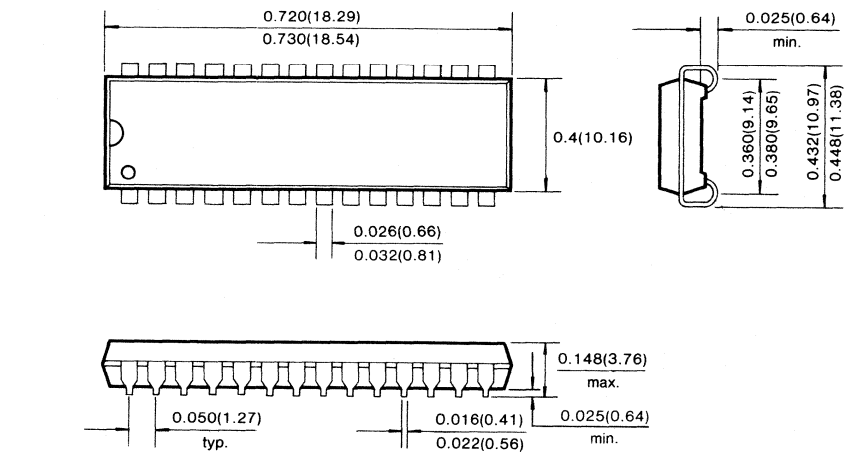
PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE (400 mil)

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE (400 mil)



262,144 WORD × 4 Bit

FEATURES

- **Fast Access Time: 10, 12ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (max.)**
  - **(CMOS): 10mA (max.)**
  - **Operating KM64B1002J-10: 150mA (max.)**
  - **KM64B1002J-12: 140mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  - **KM64B1002J: 28-pin SOJ (400 mil)**

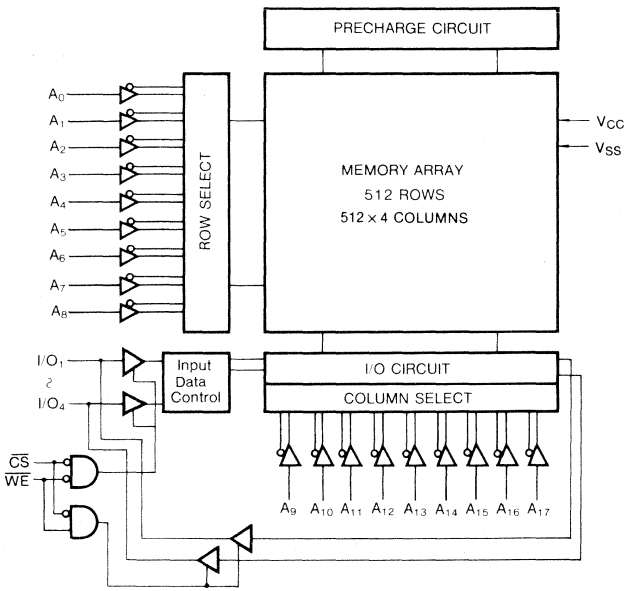
GENERAL DESCRIPTION

The KM64B1002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

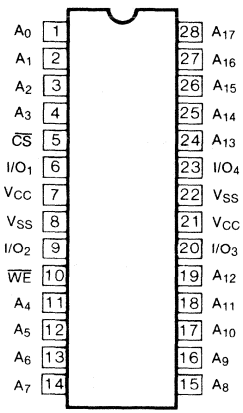
The KM64B1002 uses four common input and output lines. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high-speed system applications.

The KM64B1002 is packaged in a 400 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −2.0V ac (pulse width ≤ 10ns) for I ≤ 20mA
** V_{IH} (max.) = V_{CC} + 2V ac (pulse width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{OUT} = V_{SS}$ to V_{CC}		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	10ns	—	150	mA
			12ns	—	140	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}/V_{IL}$, Min. Cycle		—	60	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$		—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

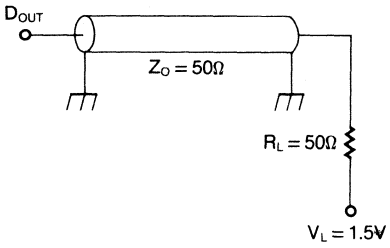
Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

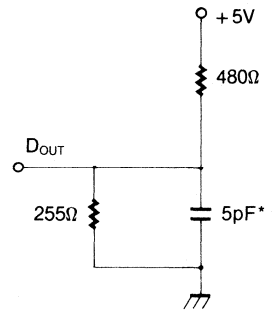
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{OW}, t_{LZ} & t_{WZ})



* Including Scope and Jig Capacitance

READ CYCLE

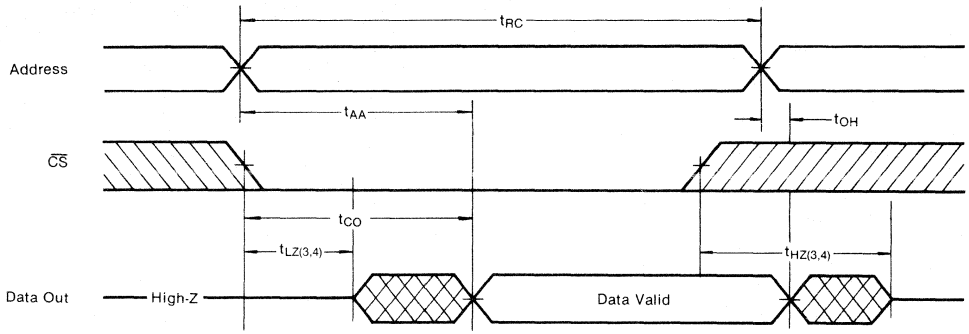
Parameter	Symbol	KM64B1002-10		KM64B1002-12		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10		12		ns
Address Access Time	t_{AA}		10		12	ns
Chip Select to Output	t_{CO}		10		12	ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		ns
Chip Disable to High-Z Output	t_{HZ}		5		6	ns
Output Hold from Address Change	t_{OH}	3		3		ns

WRITE CYCLE

Parameter	Symbol	KM64B1002-10		KM64B1002-12		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10		12		ns
Chip Select to End of Write	t_{CW}	7		8		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	7		8		ns
Write Pulse Width	t_{WP}	7		8		ns
Write Recovery Time	t_{WR}	1		1		ns
Write to Output High-Z	t_{WZ}		5		6	ns
Data to Write Time Overlap	t_{DW}	5		6		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	4		4		ns

TIMING DIAGRAMS

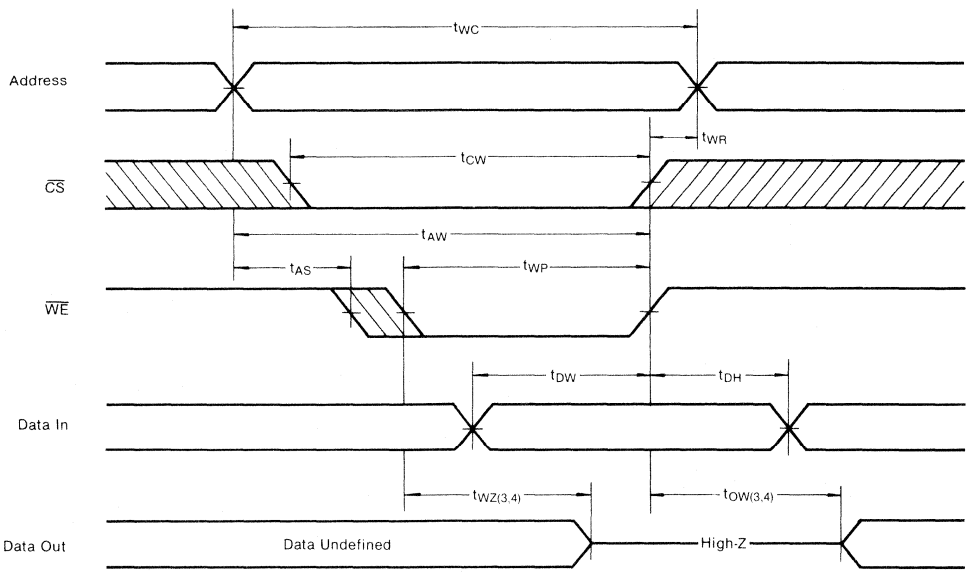
TIMING WAVEFORM OF READ CYCLE



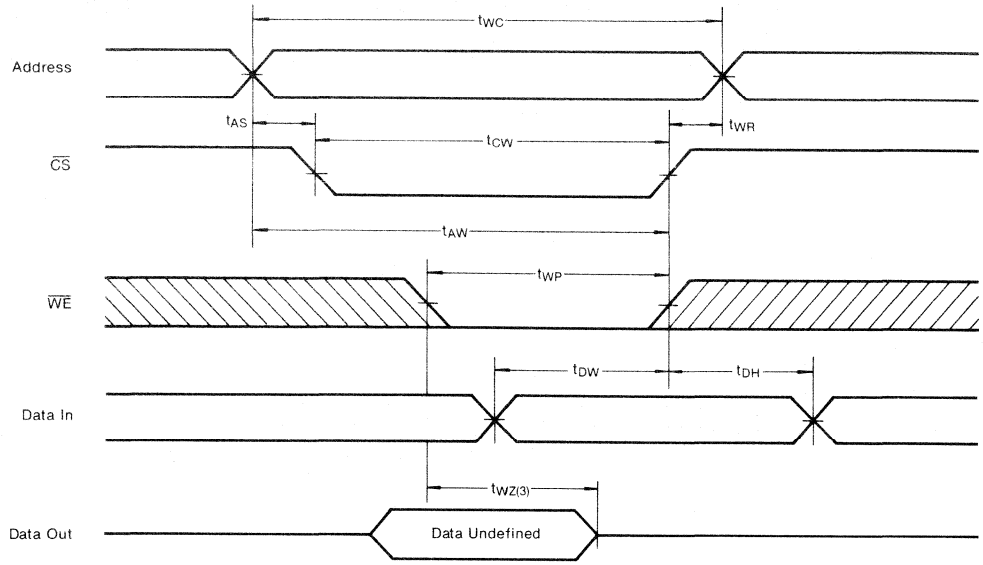
Notes (Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measuled ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (Write Cycle)

1. A write occures during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ± 200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.

FUNCTIONAL DESCRIPTION

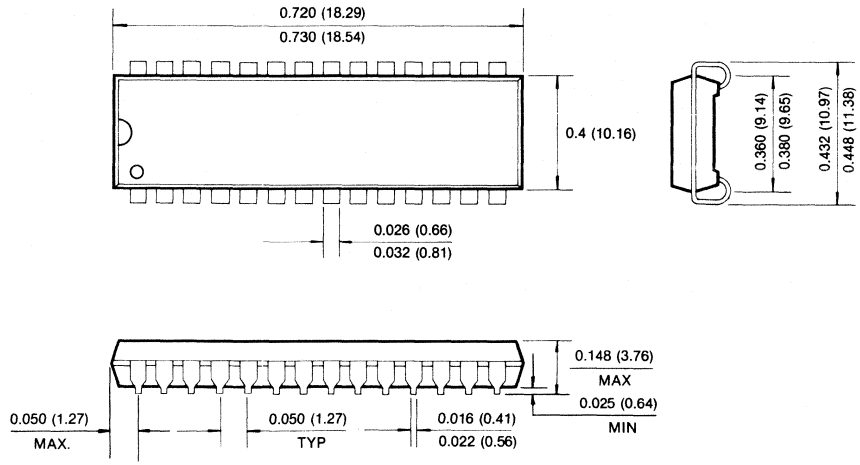
$\overline{CS}$	$\overline{WE}$	I/O Pin	Supply Current	Mode
H	X*	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	D_{OUT}	I_{CC}	Read
L	L	D_{IN}	I_{CC}	Write

* Note: X means Don't Care.

PACKAGE DIMENSIONS

28 LEAD PLASTIC SMALL OUT LINE J FORM PACKAGE

Unit: Inches (millimeters)



262,144 WORD × 4 Bit (With $\overline{OE}$)

FEATURES

- **Fast Access Time: 10, 12ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (max.)**
  - **(CMOS): 10mA (max.)**
  - **Operating KM64B1003J-10: 150mA (max.)**
  - **KM64B1003J-12: 140mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  - **KM64B1003J: 32-pin SOJ (400 mil)**

GENERAL DESCRIPTION

The KM64B1003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits.

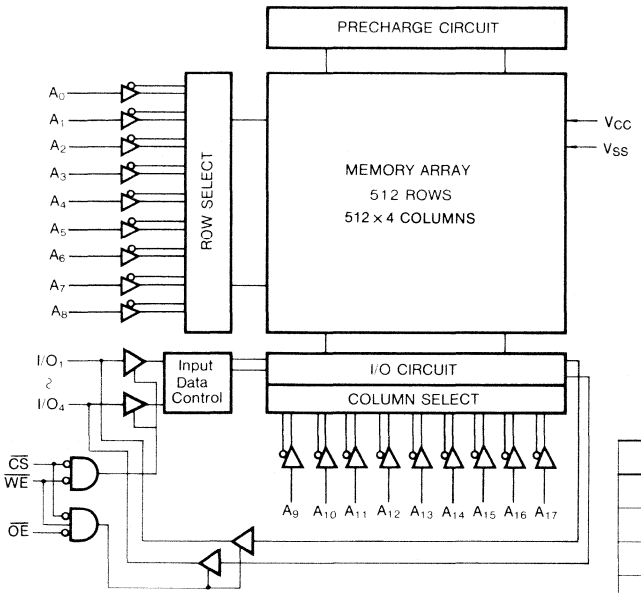
The KM64B1003 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high-speed system applications.

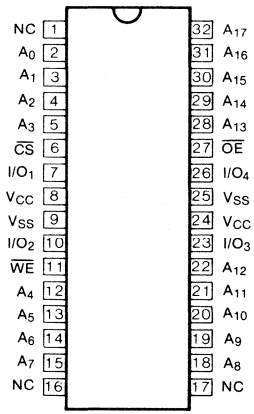
The KM64B1003 is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IH} (min.) = −2.0V ac (pulse width ≤ 10ns) for I ≤ 20mA
** V_{IL} (max.) = V_{CC} + 2V ac (pulse width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = V_{SS}$ to V_{CC}		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	10ns	—	150	mA
			12ns	—	140	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}/V_{IL}$, Min. Cycle		—	60	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

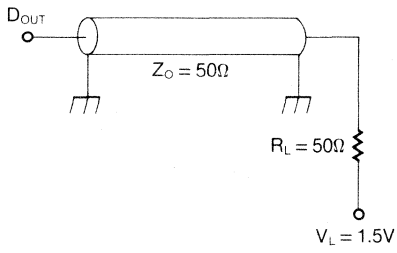
Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

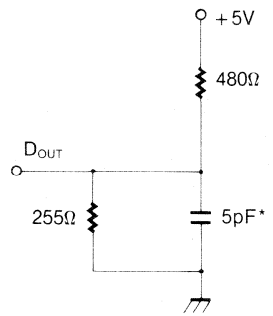
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including Scope and Jig Capacitance

READ CYCLE

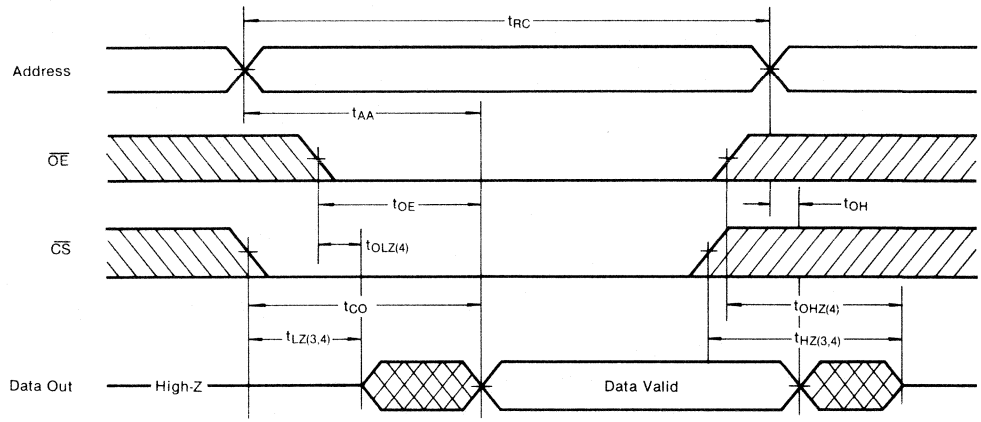
Parameter	Symbol	KM64B1003-10		KM64B1003-12		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10		12		ns
Address Access Time	t_{AA}		10		12	ns
Chip Select to Output	t_{CO}		10		12	ns
Output Enable to Output	t_{OE}		5		6	ns
Output Enable to Low-Z Output	t_{OLZ}	1		1		ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		ns
Output Disable to High-Z Output	t_{OHZ}		5		6	ns
Chip Disable to High-Z Output	t_{HZ}		5		6	ns
Output Hold from Address Change	t_{OH}	3		3		ns

WRITE CYCLE

Parameter	Symbol	KM64B1003-10		KM64B1003-12		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10		12		ns
Chip Select to End of Write	t_{CW}	7		8		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	7		8		ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	7		8		ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8		9		ns
Write Recovery Time	t_{WR}	1		1		ns
Write to Output High-Z	t_{WZ}		5		6	ns
Data to Write Time Overlap	t_{DW}	5		6		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	4		4		ns

TIMING DIAGRAMS

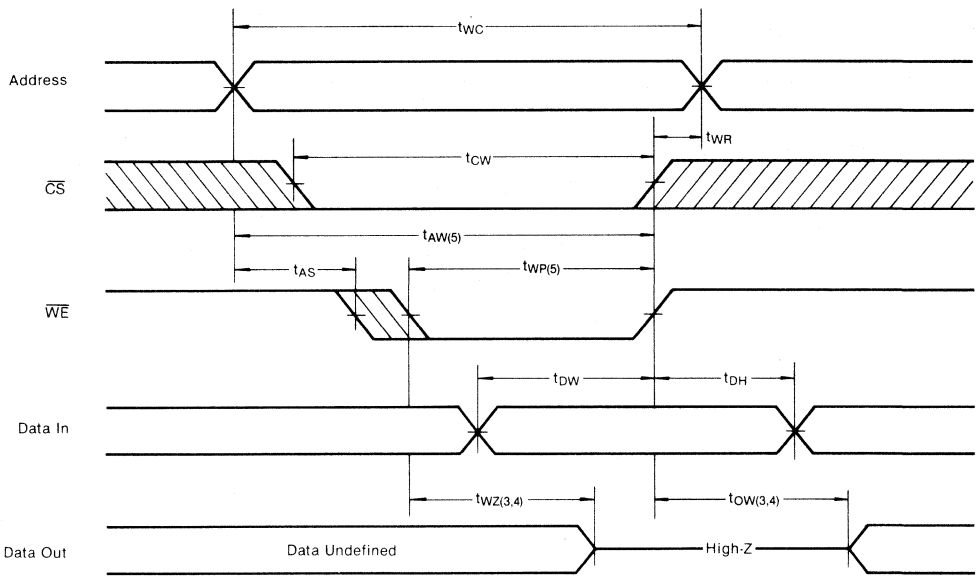
TIMING WAVEFORM OF READ CYCLE



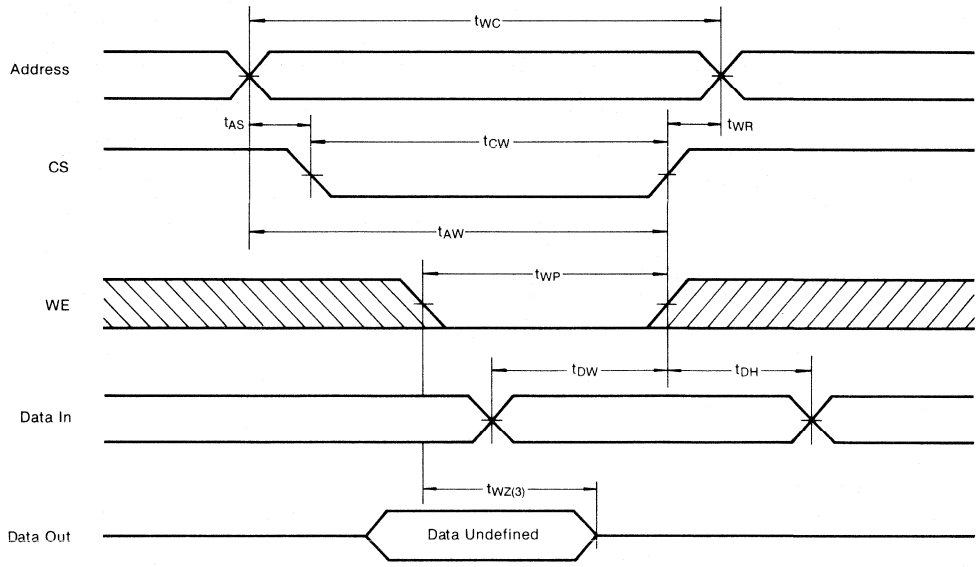
Notes (Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measuled ±200mV from steady state voltage with Load (B).
   This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (Write Cycle)

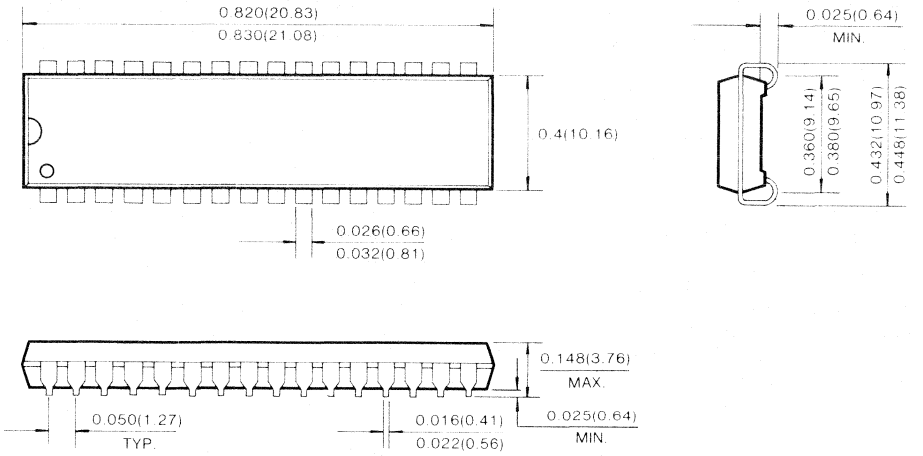
1. A write occures during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. The min. t_{AW} and t_{WP} for write cycle with $\overline{OE}$ low is the sum of t_{WZ} and t_{DW}.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

32 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE (400 mil)



256KX4 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time 20,25,35ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA (max.)**
  - **Operating KM641005P/J-20: 150mA (max)**
  - **KM641005P/J-25: 130mA (max)**
  - **KM641005P/J-35: 110mA (max)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **-No clock or refresh required**
- **Three State Output**
- **Standard Pin Configuration**
  - **KM641005P: 32-pin DIP (400mil)**
  - **KM641005J: 32-pin SOJ (400mil)**

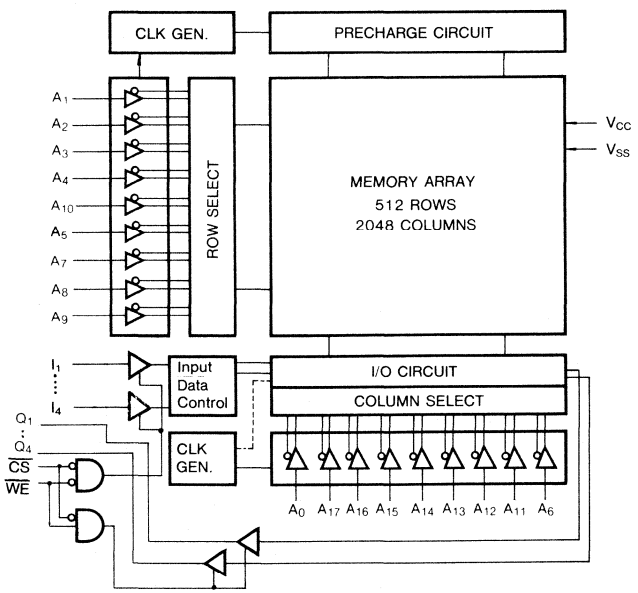
GENERAL DESCRIPTION

The KM641005 is a 1,048,576-bit high-speed static random access memory organized as 262,144 words by 4 bit.

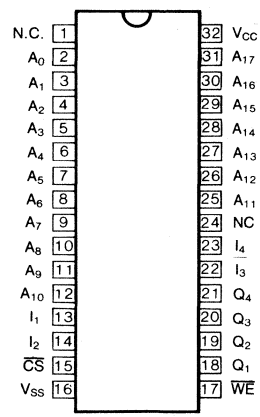
The KM641005 has seperate input and output lines for fast read and write access. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM641005 is packaged in a 400mil 32-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A0-A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I_1-I_4	Data Inputs
Q_1-Q_4	Data Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty	20ns		150	mA
		$\overline{CS}$=V_{IL}, I_{OUT}=0mA	25ns		130	mA
			35ns		110	mA
Standby Power Supply Current	I_{sb}	$\overline{CS}$=V_{IH}			40	mA
	I_{sb1}	$\overline{CS}$≥V_{CC}-0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA		2.4		V

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	7	pF

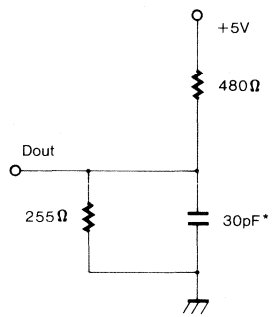
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

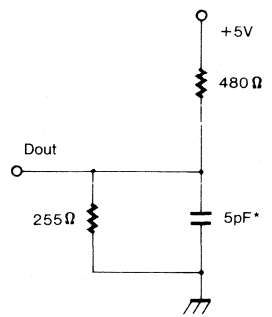
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641005-20		KM641005-25		KM641005-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO}		20		25		35	ns
Chip Enable to Low-Z Output	t_{LZ}	0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}		20		25		35	ns

WRITE CYCLE

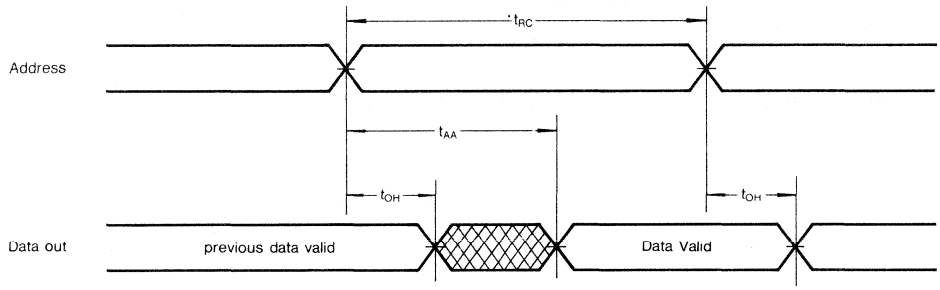
Parameter	Symbol	KM641005-20		KM641005-25		KM641005-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Write Pluse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

2

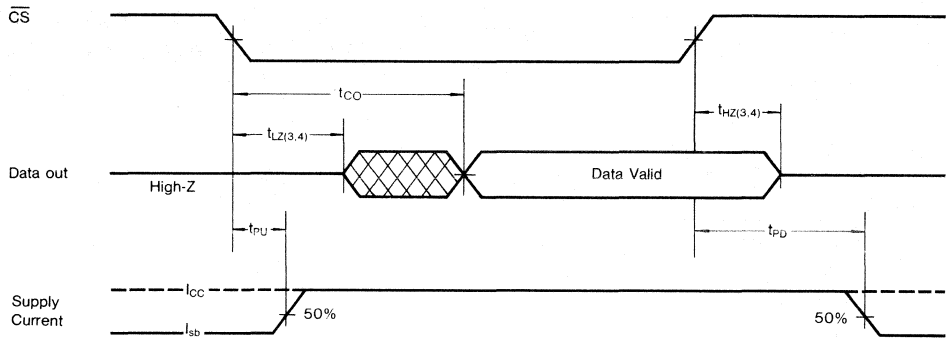
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS} = V_{IL}$, $\overline{WE} = V_{IH}$)



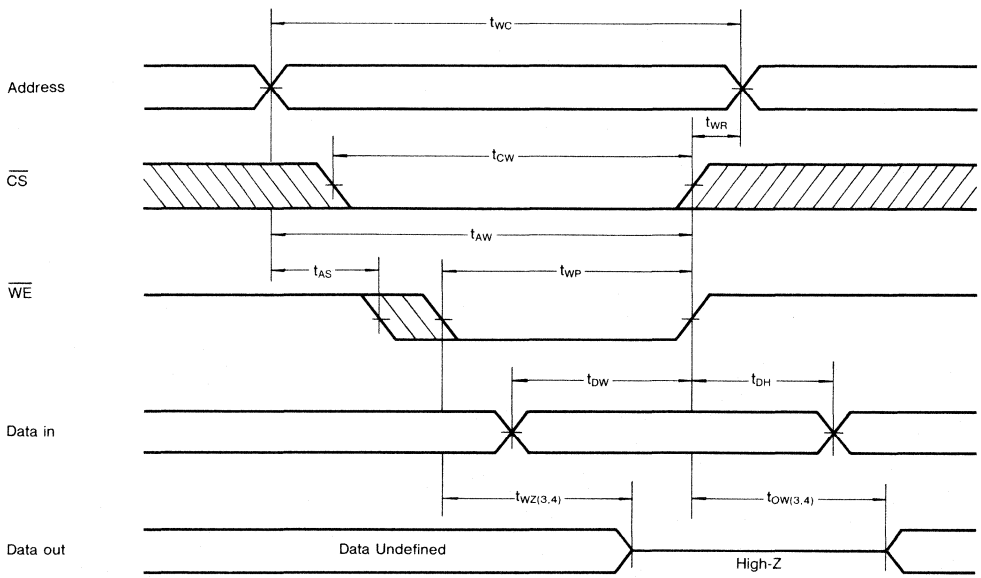
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



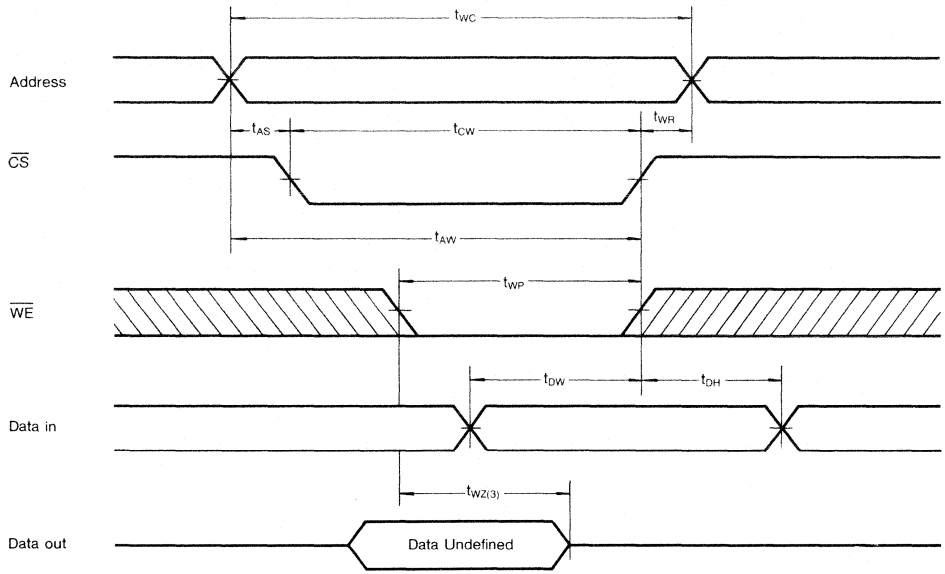
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

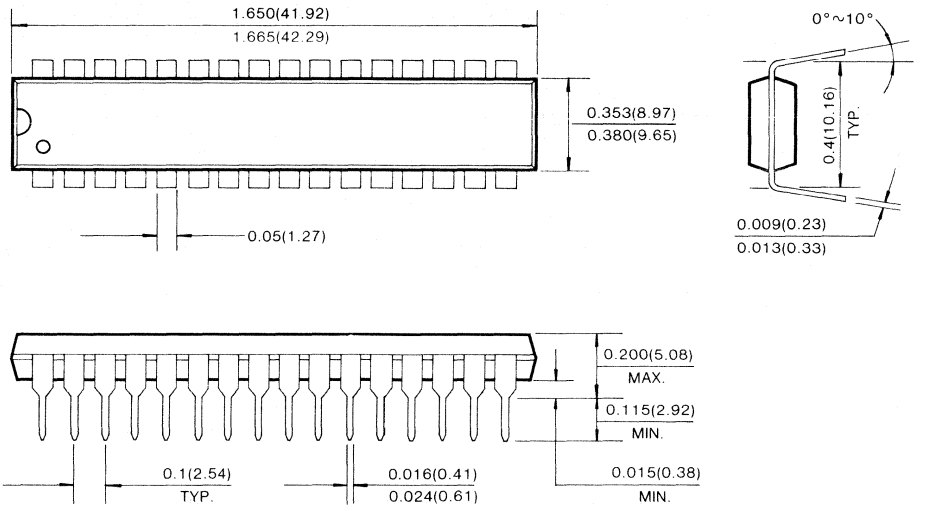
$\overline{CS}$	$\overline{WE}$	Dout PIN	Supply Current	Mode
H	X*	High-Z	I_{sb}, I_{sb1}	Not Select
L	H	Dout	I_{CC}	Read
L	L	High-Z	I_{CC}	Write

*Note: X means Don't Care

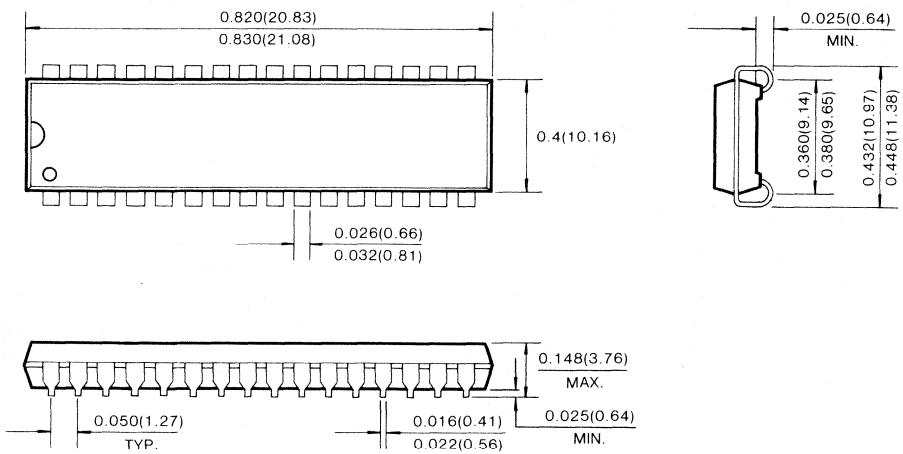
PACKAGES DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (400 mil)

Unit: Inches (Millimeters)



32 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE (400 mil)



128KX8 Bit High-Speed Static RAM

FEATURES

- **Fast Access Time 20,25,35ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 40mA (max.)**
  - **(CMOS) : 2mA (max.)**
  - **Operating KM681001P/J-20: 170mA (max.)**
  - **KM681001P/J-25: 150mA (max.)**
  - **KM681001P/J-35: 130mA (max.)**
- **Single 5V±10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **-No clock or refresh required**
- **Three state Output**
- **Standard Pin Configuration**
  - **KM681001P: 32-pin DIP (400mil)**
  - **KM681001J: 32-pin SOJ (400mil)**

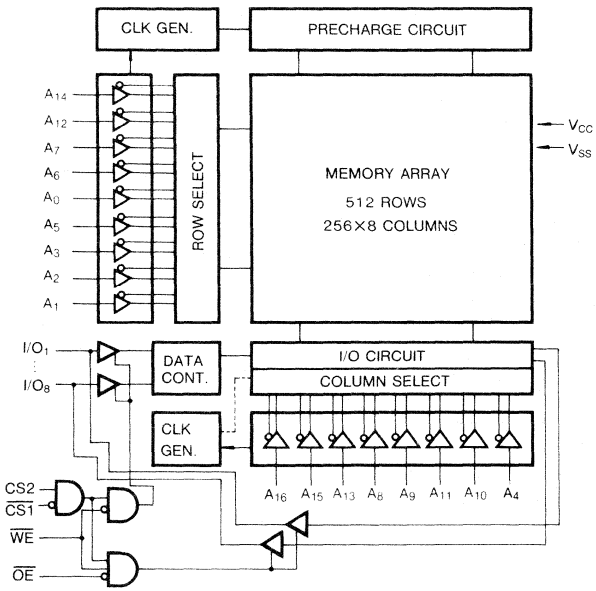
GENERAL DESCRIPTION

The KM681001 is a 1,048,576-bit high-speed static random access memory organized as 131,072 words by 8 bit.

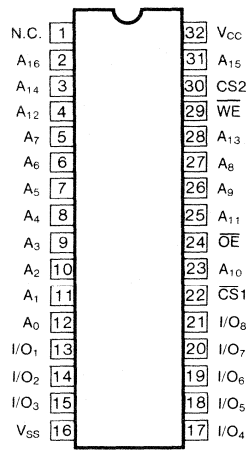
The KM681001 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high speed system applications.

The KM681001 is packaged in a 400mil 32-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A0-A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS_1}$, CS_2	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	$V_{in, out}$	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	Pd	1.0	W
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL}(min.)=−3.0V for≤10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}			2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=V_{SS} to V_{CC}			2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty	20ns		170	mA
		$\overline{CS1}$=V_{IL}, CS2=V_{IH}	25ns		150	mA
		$I_{I/O}$=0mA	35ns		130	mA
Standby Power Supply Current	I_{sb}	$\overline{CS1}$=V_{IH} or CS2=V_{IL}			40	mA
	I_{sb1}	$\overline{CS1}$≥V_{CC}-0.2V CS2≥V_{CC}-0.2V or CS2≤0.2V V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V			2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA		2.4		V

CAPACITANCE (f=1Mhz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

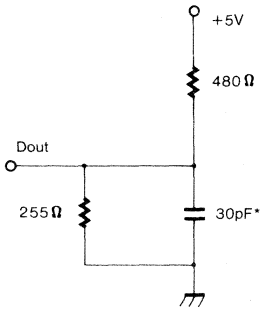
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

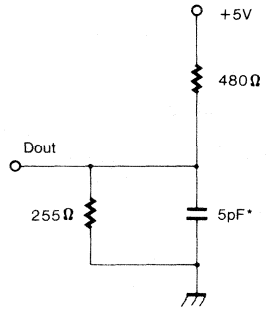
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



*Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681001-20		KM681001-25		KM681001-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO1}, t_{CO2}		20		25		35	ns
Output Enable to Output	t_{OE}		10		13		15	ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	0		0		0		ns
Output Disable to High-Z Output	t_{OHZ}	0	8	0	10		15	
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns

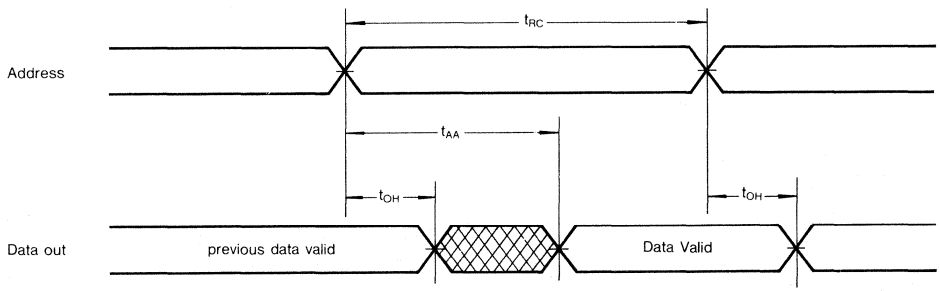
WRITE CYCLE

Parameter	Symbol	KM681001-20		KM681001-25		KM681001-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Write Pluse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

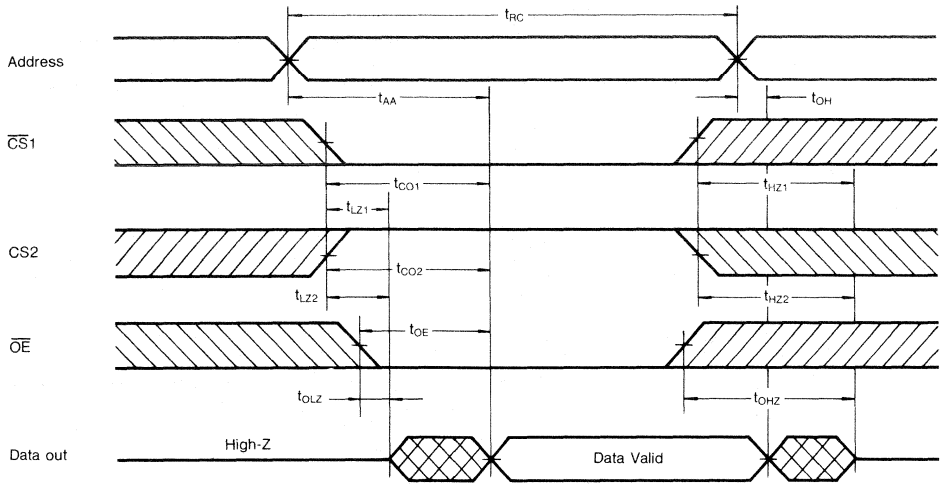
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}1=\overline{OE}=V_{IL}$, $CS2=V_{IH}$, $\overline{WE}=V_{IH}$)



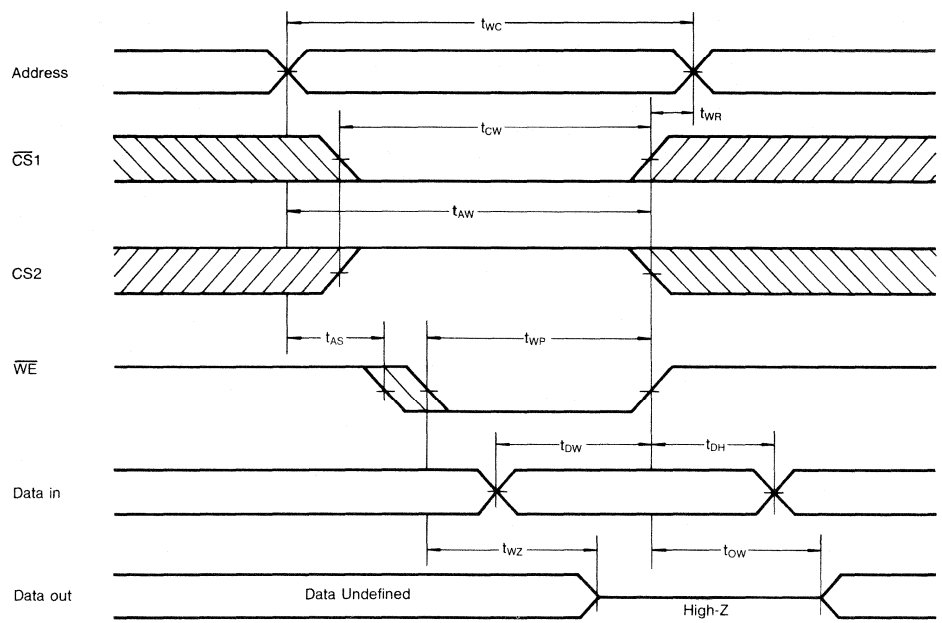
TIMING WAVEFORM OF READ CYCLE



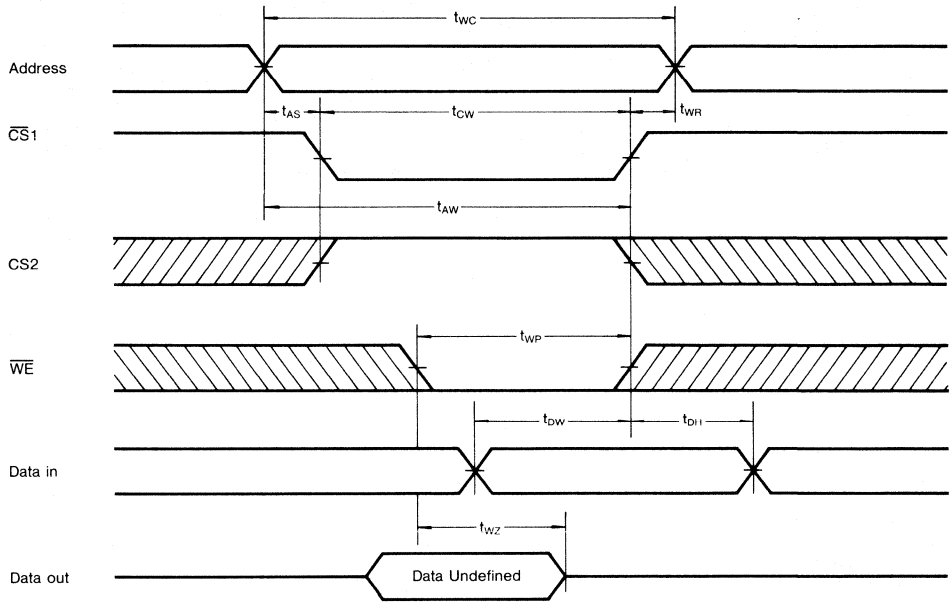
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
3. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min).

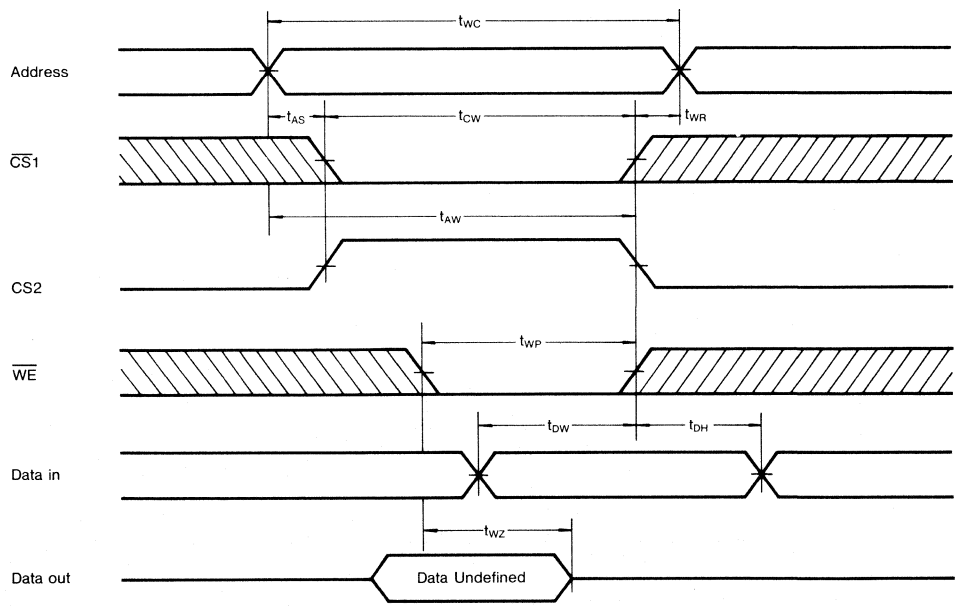
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and WE going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{CS1}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

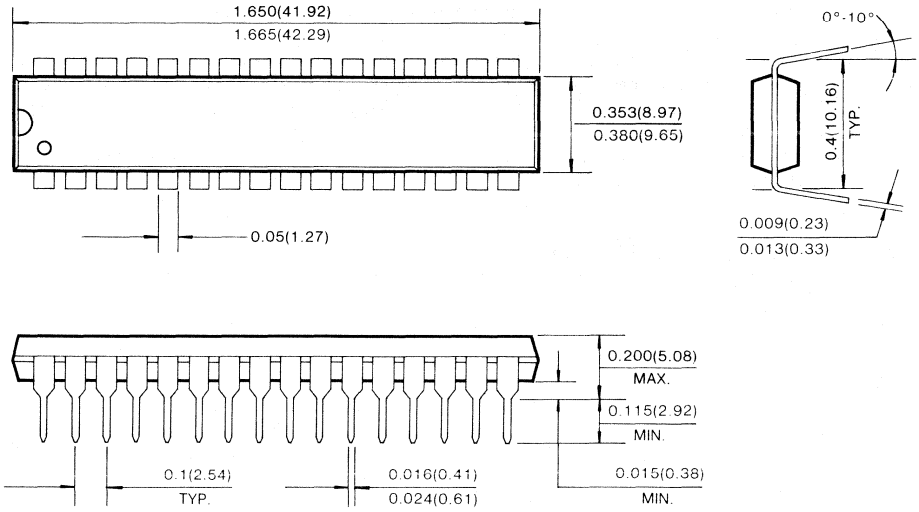
$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

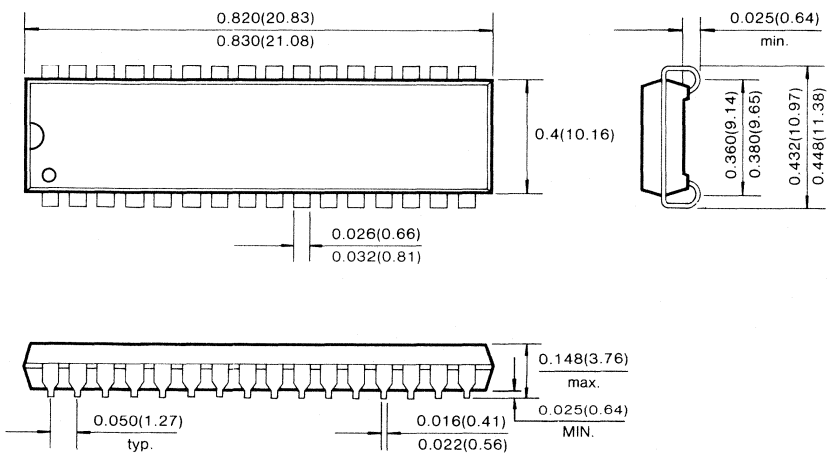
PACKAGES DIMENSIONS

32 PIN PLASTIC DUAL IN LINE PACKAGE (400 mil)

Unit: Inches (Millimeters)



32 PIN PLASTIC SMALL OUT LINE J FORM PACKAGE (400 mil)



131,072 WORD × 8 Bit

FEATURES

- **Fast Access Time: 10, 12ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (max.)**
  - **(CMOS): 10mA (max.)**
  - **Operating KM68B1002J-10: 160mA (max.)**
  - **KM68B1002J-12: 150mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Center Power/Ground Pin Configuration**
- **Standard Pin Configuration**
  - **KM68B1002J: 32-pin SOJ (400 mil)**

GENERAL DESCRIPTION

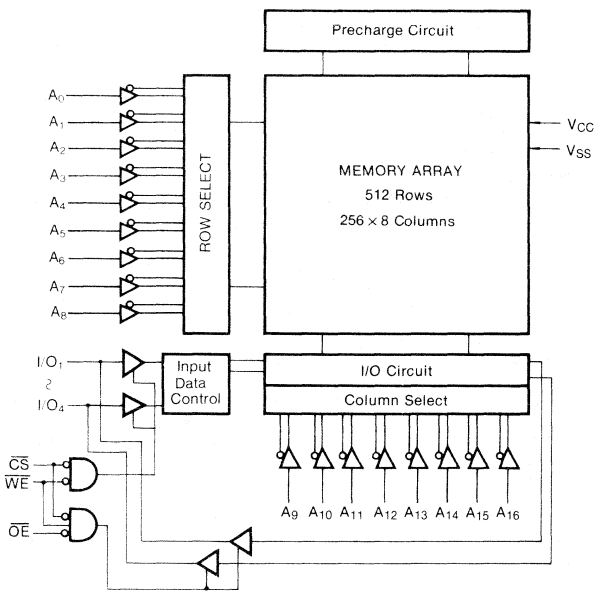
The KM68B1002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits.

The KM68B1002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high-speed system applications.

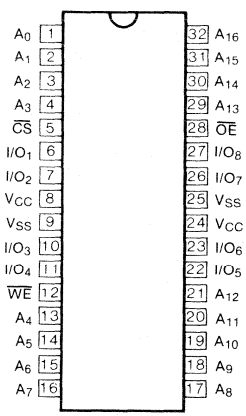
The KM68B1002 is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IH} (min.) = −2.0V ac (pulse width ≤ 10ns) for I ≤ 20mA
** V_{IL} (max.) = V_{CC} + 2V ac (pulse width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{OUT} = V_{SS}$ to V_{CC}		—	10	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS} = V_{IL}$, I_{OUT} = 0mA	10ns	—	160	mA
			12ns	—	150	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}/V_{IL}$, Min. Cycle		—	60	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$		—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

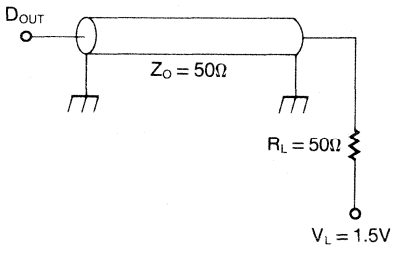
Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

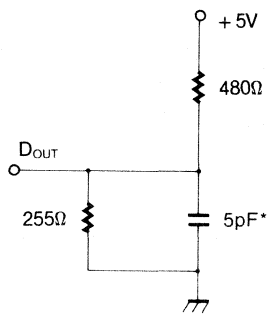
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{OW} & t_{WZ})



* Including Scope and Jig Capacitance

READ CYCLE

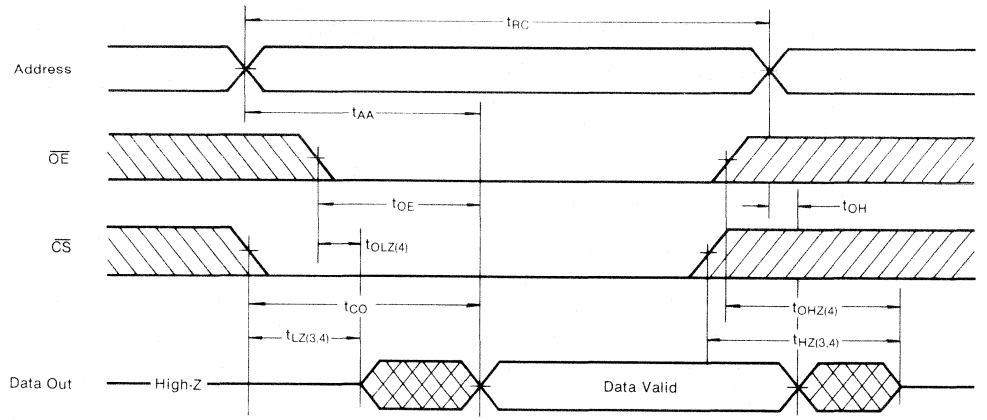
Parameter	Symbol	KM68B1002-10		KM68B1002-12		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10		12		ns
Address Access Time	t_{AA}		10		12	ns
Chip Select to Output	t_{CO}		10		12	ns
Output Enable to Valid Output	t_{OE}		5		6	ns
Output Enable to Low-Z Output	t_{OLZ}	1		1		ns
Chip Enable to Low-Z Output	t_{LZ}	3		3		ns
Output Disable to High-Z Output	t_{OHZ}		5		6	ns
Chip Disable to High-Z Output	t_{HZ}		5		6	ns
Output Hold from Address Change	t_{OH}	3		3		ns

WRITE CYCLE

Parameter	Symbol	KM68B1002-10		KM68B1002-12		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10		12		ns
Chip Select to End of Write	t_{CW}	7		8		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	7		8		ns
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	7		8		ns
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}	8		9		ns
Write Recovery Time	t_{WR}	1		1		ns
Write to Output High-Z	t_{WZ}		5		6	ns
Data to Write Time Overlap	t_{DW}	5		6		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Output Low-Z	t_{OW}	4		4		ns

TIMING DIAGRAMS

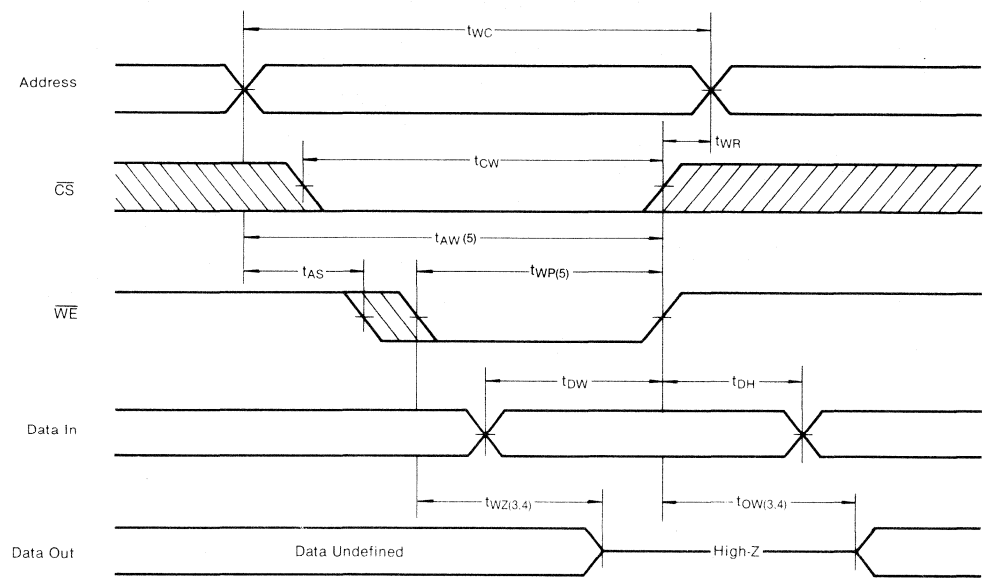
TIMING WAVEFORM OF READ CYCLE



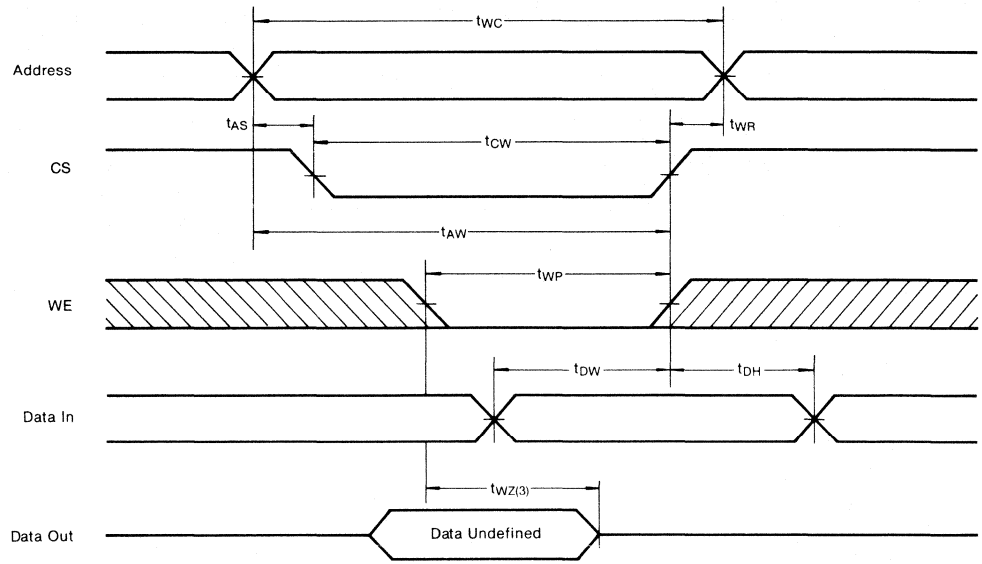
Notes (Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
4. Transition is measuled ±200mV from steady state voltage with Load (B).
   This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (Write Cycle)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. The min. t_{AW} and t_{WP} for write cycle with $\overline{OE}$ low is the sum of t_{WZ} and t_{DW}.

FUNCTIONAL DESCRIPTION

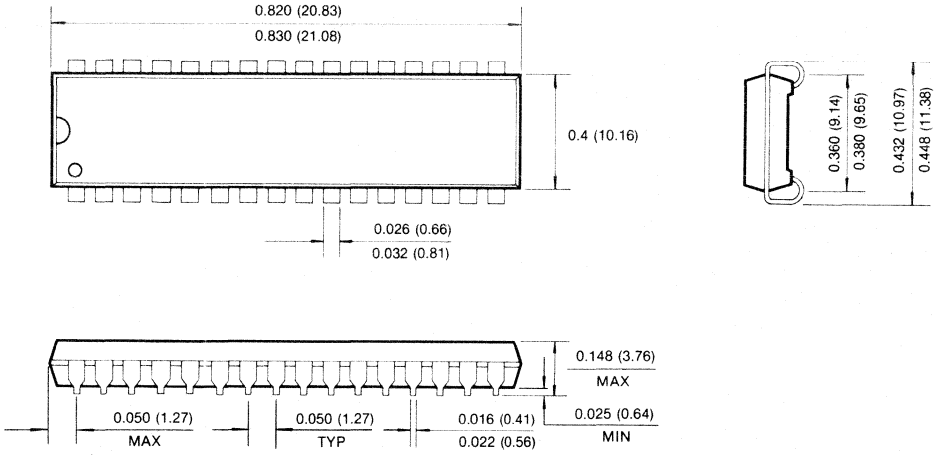
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

PACKAGE DIMENSIONS

32 LEAD PLASTIC SMALL OUT LINE J FORM PACKAGE

Unit: Inches (millimeters)



1,048,576 WORD x 4 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM644002J-15: 180mA (max.)**
  - **KM644002J-20: 160mA (max.)**
  - **KM644002J-25: 140mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM644002J: 32-pin SOJ (400 mil)**

GENERAL DESCRIPTION

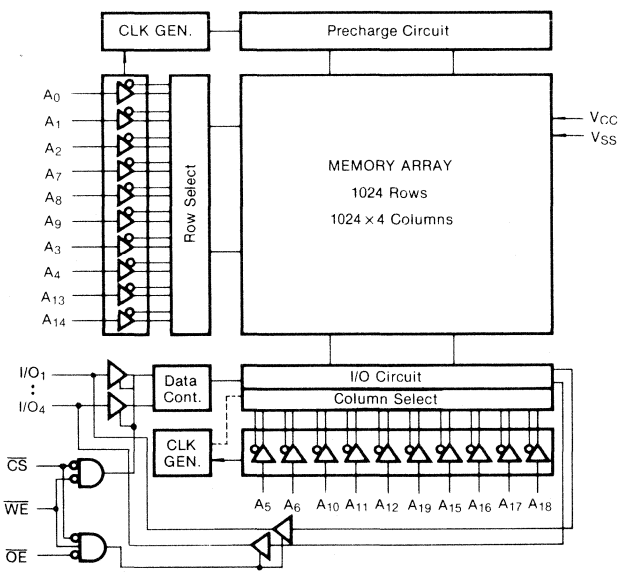
The KM644002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

The KM644002 uses four common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

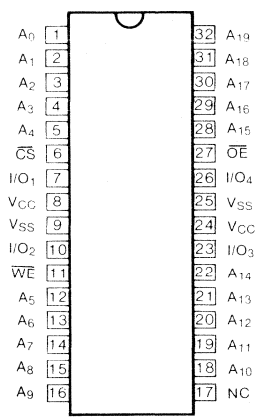
It is particularly well suited for use in high-density high-speed system applications.

The KM644002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

1,048,576 WORD × 4 Bit Separate I/O High Speed CMOS Static RAM

FEATURES

- Fast Access Time: 15, 20, 25ns (max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA (max.)
  - (CMOS): 20mA (max.)
  - Operating KM644005J-15: 180mA (max.)
  - KM644005J-20: 160mA (max.)
  - KM644005J-25: 140mA (max.)
- Single 5V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No clock or refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM644005J: 36-pin SOJ (400 mil)

GENERAL DESCRIPTION

The KM644005 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits.

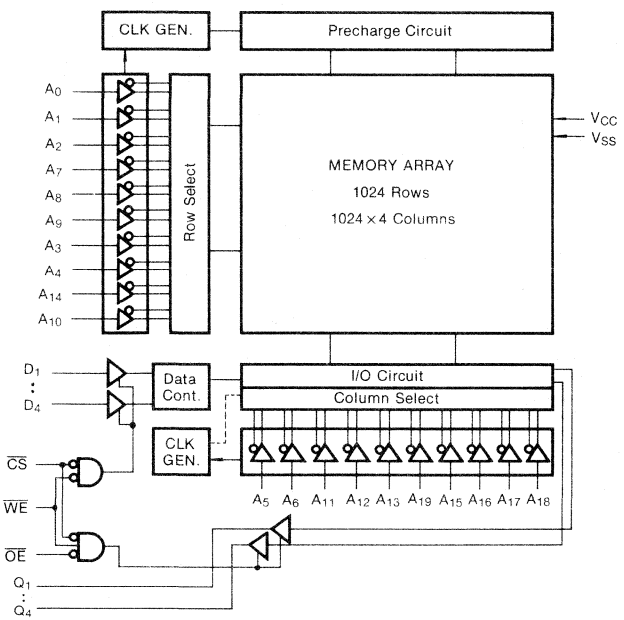
The KM644005 has seperate input and output lines for fast read and write access. The data output pins stay in High-Z state when write enable is low or chip select is high. The devices is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications.

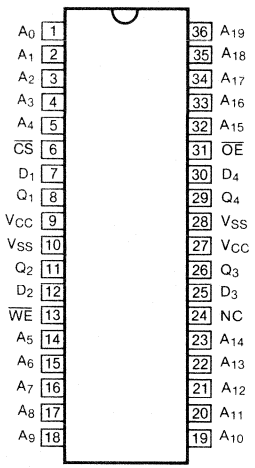
The KM644005 is packaged in a 400 mil 36-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{19}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
OE	Output Enable
D_1-D_4	Data Inputs
Q_1-Q_4	Data Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

524,288 WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM644005J-15: 180mA (max.)**
  - **KM644005J-20: 160mA (max.)**
  - **KM644005J-25: 140mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM684002J: 36-pin SOJ (400 mil)**

GENERAL DESCRIPTION

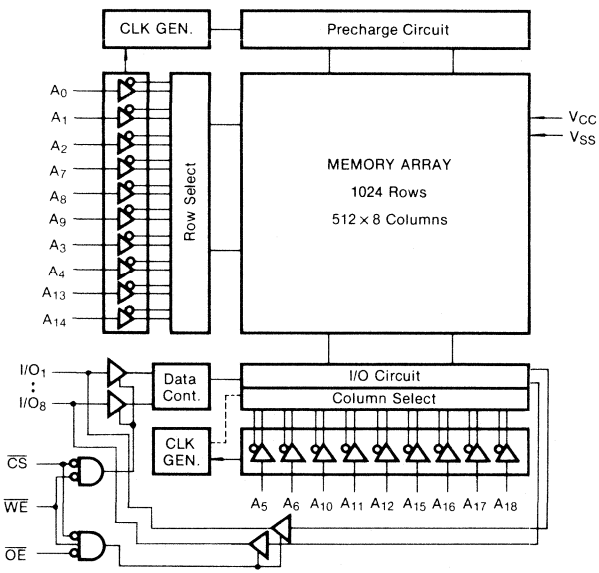
The KM684002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits.

The KM684002 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

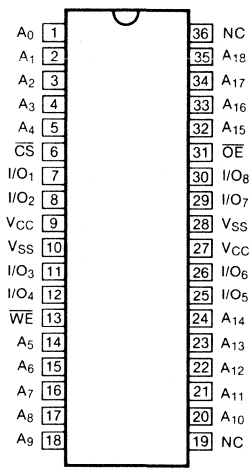
It is particularly well suited for use in high-density high-speed system applications.

The KM684002 is packaged in a 400 mil 36-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{18}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

262,144 WORD × 16 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time: 15, 20, 25ns (max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 60mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM6164002J-15: 280mA (max.)**
  - **KM6164002J-20: 260mA (max.)**
  - **KM6164002J-25: 240mA (max.)**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three State Outputs**
- **Data Byte Control : $\overline{LB}$: $I/O_1 \sim I/O_8$**
  - **$\overline{UB}$: $I/O_9 \sim I/O_{16}$**
- **Standard Pin Configuration**
  - **KM6164002J: 44-pin SOJ (400 mil)**

GENERAL DESCRIPTION

The KM6164002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits.

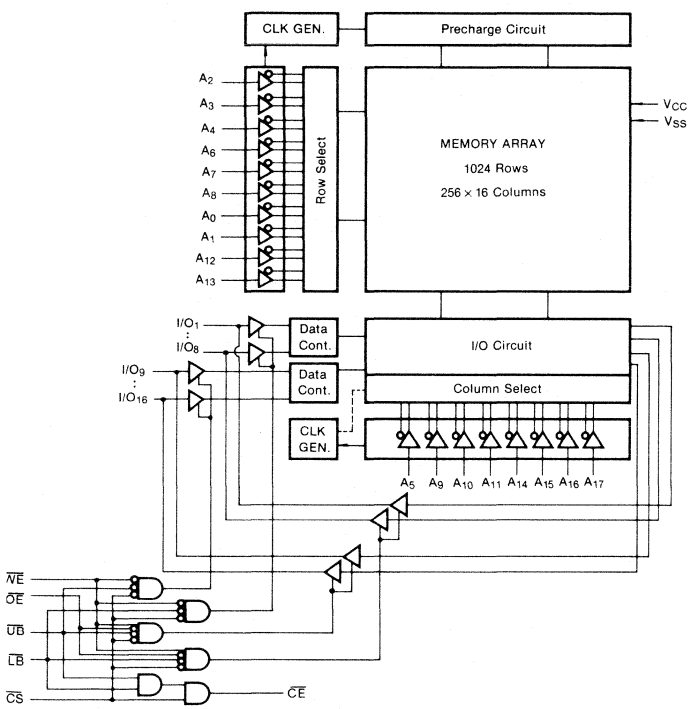
The KM6164002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{LB}$, $\overline{UB}$). The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

It is particularly well suited for use in high-density high-speed system applications.

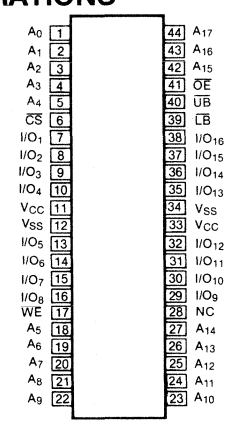
The KM6164002 is packaged in a 400 mil 44-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



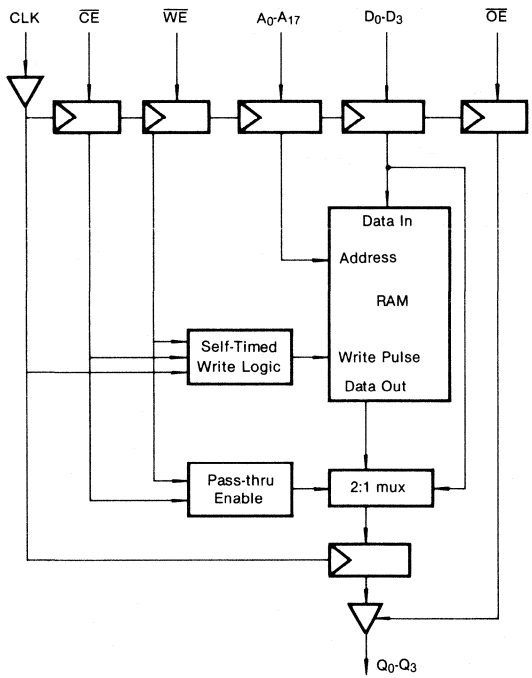
Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control ($I/O_1 \sim I/O_8$)
$\overline{UB}$	Upper-byte Control ($I/O_9 \sim I/O_{16}$)
I/O_1-I/O_{16}	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

262,144 Words x 4-Bit Synchronous Static Random Access Memory

FEATURES

- **Fast Cycle Time: 12,5ns (Max.)**
- **Low Power Dissipation (min. Cycle, 100% Duty)**
  KM741006J-12: 190mA
- **Single 5V ± 5% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **All Inputs and Outputs Registered with Clock**
- **Three State Outputs**
- **Available in Plastic 36 Pin 400 mil SOJ**

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Timing Reference	Pin Function
A_0-A_{17}	A	Address Input
$\overline{WE}$	W	Write Enable Input
$\overline{CE}$	E	Chip Enable Input
$\overline{OE}$	G	Output Enable Input
D_0-D_3	D	Data Input
Q_0-Q_3	Q	Data Output
CLK	C	Clock Input
V_{CC}	—	+5V Power Supply
V_{SS}	—	Ground
NC	—	No Connection

GENERAL DESCRIPTION

The KM741006J is a 1,048,576 bit synchronous high-speed SRAM organized as a 262,144 words by 4 bits. The device integrates a 256K x 4 bits SRAM core with advanced synchronous peripheral circuitry, which includes input registers, output registers, address registers and control registers.

All signals pass thru registers triggered by a positive-edge of clock input(K).

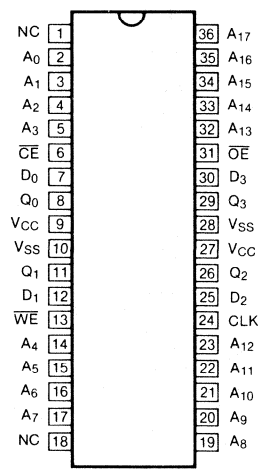
In read operation, the data of cell array accessed by the current address, registered in the address registers by the positive edge of K, are carried to the Data-out registers by the next positive edge of K. The data, registered in the Data-out registers, are projected to the output pins.

In write operation, the write data, registered in the Data-in registers, are stored in both the cell array and the Data-out registeres.

This operation is fully self-timed and exclude the complexity of the write control of general SRAM. Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$.

Note that this device does not need any intervening recovery cycles in a sequential operation of arbitrary read, write, and pass-thru cycles.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS* (T_A = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to 7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output Voltage	V_O	−0.5 to V_{CC} + 0.5	V
Allowable Power Dissipation	P_D	1.0	W
Operating Temperature	t_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	−55 to 150	°C

2

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C, GND = 0V)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.20	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.80	V

* V_{IL} = −1V Min, for 3ns per cycle.

ELECTRICAL DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, GND = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}	−2	2	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{OE}$ = V_{IH}	−2	2	μA
Average Operating Current	I_{CC}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	—	190	mA
Standby Current	I_{SB}	V_{IN} = V_{IH} or V_{IL}, DC, I_{OUT} = 0mA, $\overline{CE}$ = $\overline{WE}$ = $\overline{OE}$ = V_{IH}	—	40	mA
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	—	0.4	V

TRUTH TABLES

CLK	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Operation
↑	H	H	H	Outputs High-Z, deselect operation
↑	H	H	L	Store D_0 to D_3 in Output Registers, Outputs High-Z
↑	H	L	H	Read from Output Registers
↑	H	L	L	Pass-thru
↑	L	L	H	Read Q_0 to Q_3
↑	L	H	H	Store Q_0 to Q_3 in Output Registers, Outputs High-Z
↑	L	H	L	Write D_0 to D_3 and store in Output Registers, Output High-Z
↑	L	L	L	Write D_0 to D_3 and pass-thru

I/O CAPACITANCE ($T_A = 25°C$, f = 1MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	5	pF
Clock Input Capacitance	C_{CLK}	$V_{IN} = 0V$	—	8	pF
Output Capacitance	C_O	$V_O = 0V$	—	8	pF

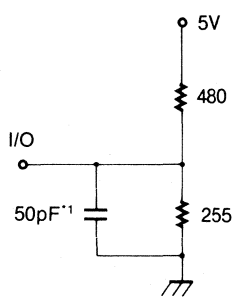
Note: This parameter is sampled and not 100% tested.

AC CHARACTERISTICS
TEST CONDITIONS

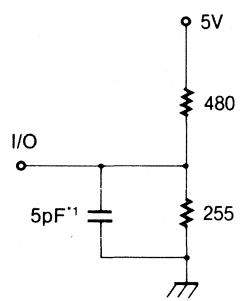
($V_{CC} = 5V \pm 5\%$, $T_A = 0$ to $+70°C$)

Item	Conditions
Input Pulse High Level	$V_{IH} = 3.0V$
Input Pulse Low Level	$V_{IL} = 0V$
Input Rise Time	$t_R = 3.0ns$
Input Fall Time	$t_F = 3.0ns$
Input Reference Level	1.5V
Output Reference Level, V_{OH}/V_{OL}	2.0/0.8V
Output Load (See test circuit in the right)	Fig. 1

Output Load (1)



Output Load (2)*2



*1 including scope and jig capacitance
*2 for T_{CHQHZ}, T_{CHQLZ}

Fig. 1

READ CYCLE

Item	Symbol	KM741006J-12		Unit
		Min	Max	
Clock cycle time	t_{CHCH}	12.5	—	ns
Clock high pulse width	t_{CH}	4.0	—	ns
Clock low pulse width	t_{CL}	4.0	—	ns
Clock high to data valid	t_{CHQV}	2.0	7	ns
Address setup to clock high	t_{AVCH}	2.0	—	ns
Address hold from clock high	t_{CHAX}	1.0	—	ns
Chip enable setup to clock high	t_{EVCH}	2.0	—	ns
Chip enable hold from clock high	t_{CHEX}	1.0	—	ns
Write enable setup to clock high	t_{WVCH}	2.0	—	ns
Write enable hold from clock high	t_{CHWX}	1.0	—	ns
Output enable setup to clock high	t_{GVCH}	2.0	—	ns
Output enable hold from clock high	t_{CHGX}	1.0	—	ns
Output hold from clock high	t_{CHQX}	2.0	—	ns
*Clock high to output low-Z	t_{CHQLZ}	2.0	7	ns
*Clock high to output high-Z	t_{CHQHZ}	2.0	10	ns

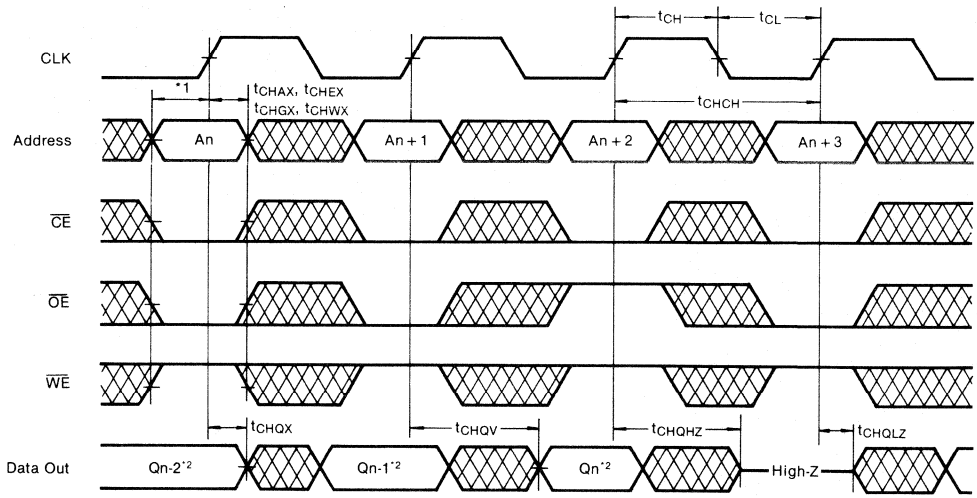
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and not 100% tested.

WRITE CYCLE AND PASS-THRU

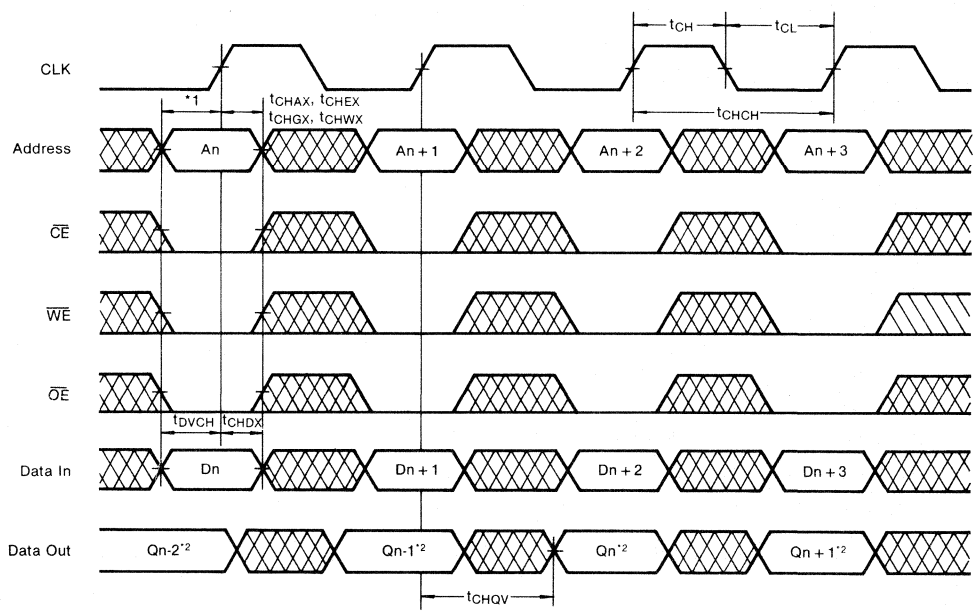
Item	Symbol	KM741006J-12		Unit
		Min	Max	
Clock cycle time	t_{CHCH}	12.5	—	ns
Clock high pulse width	t_{CH}	4.0	—	ns
Clock low pulse width	t_{CL}	4.0	—	ns
Address setup to clock high	t_{AVCH}	2.0	—	ns
Address hold from clock high	t_{CHAX}	1.0	—	ns
Chip enable setup to clock high	t_{EVCH}	2.0	—	ns
Chip enable hold from clock high	t_{CHEX}	1.0	—	ns
Write enable setup to clock high	t_{WVCH}	2.0	—	ns
Write enable hold from clock high	t_{CHWX}	1.0	—	ns
Input data setup to clock high	t_{DVCH}	2.0	—	ns
Input data hold from clock high	t_{CHDX}	1.0	—	ns

TIMING WAVEFORM

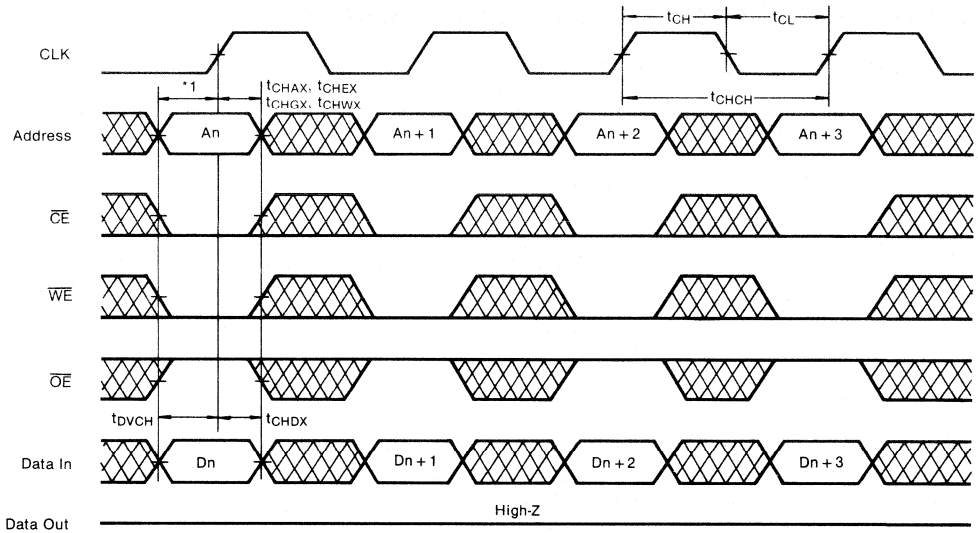
READ CYCLE:



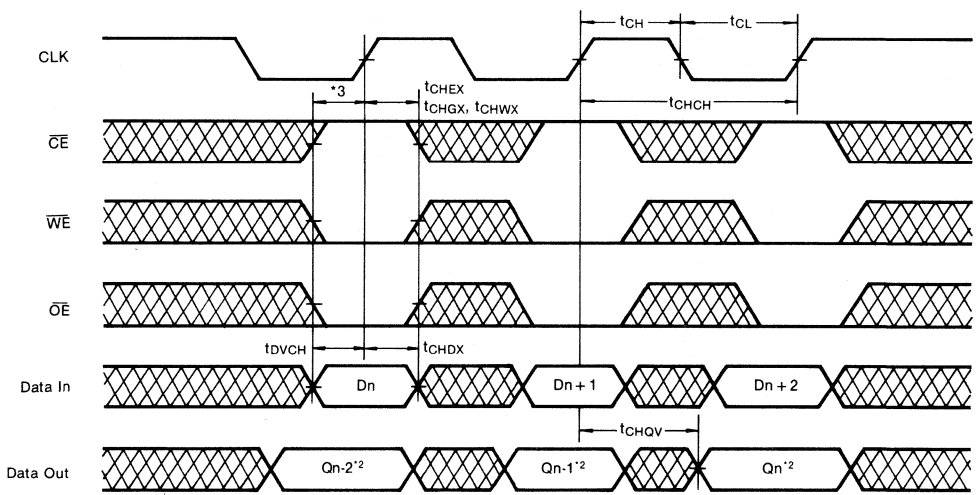
WRITE AND PASS-THRU CYCLE



WRITE CYCLE



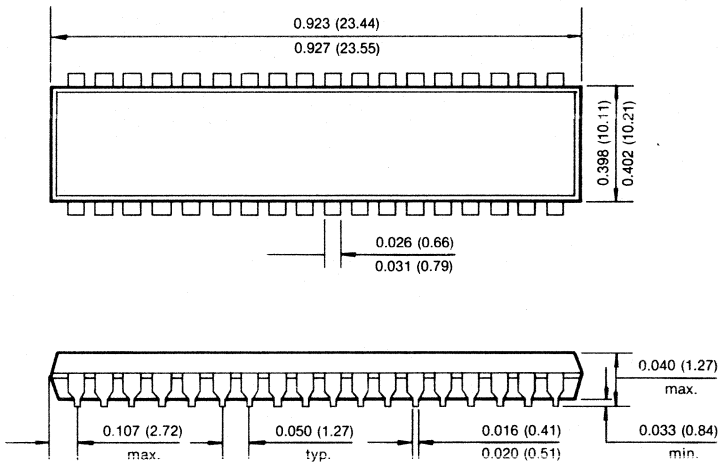
PASS-THRU CYCLE

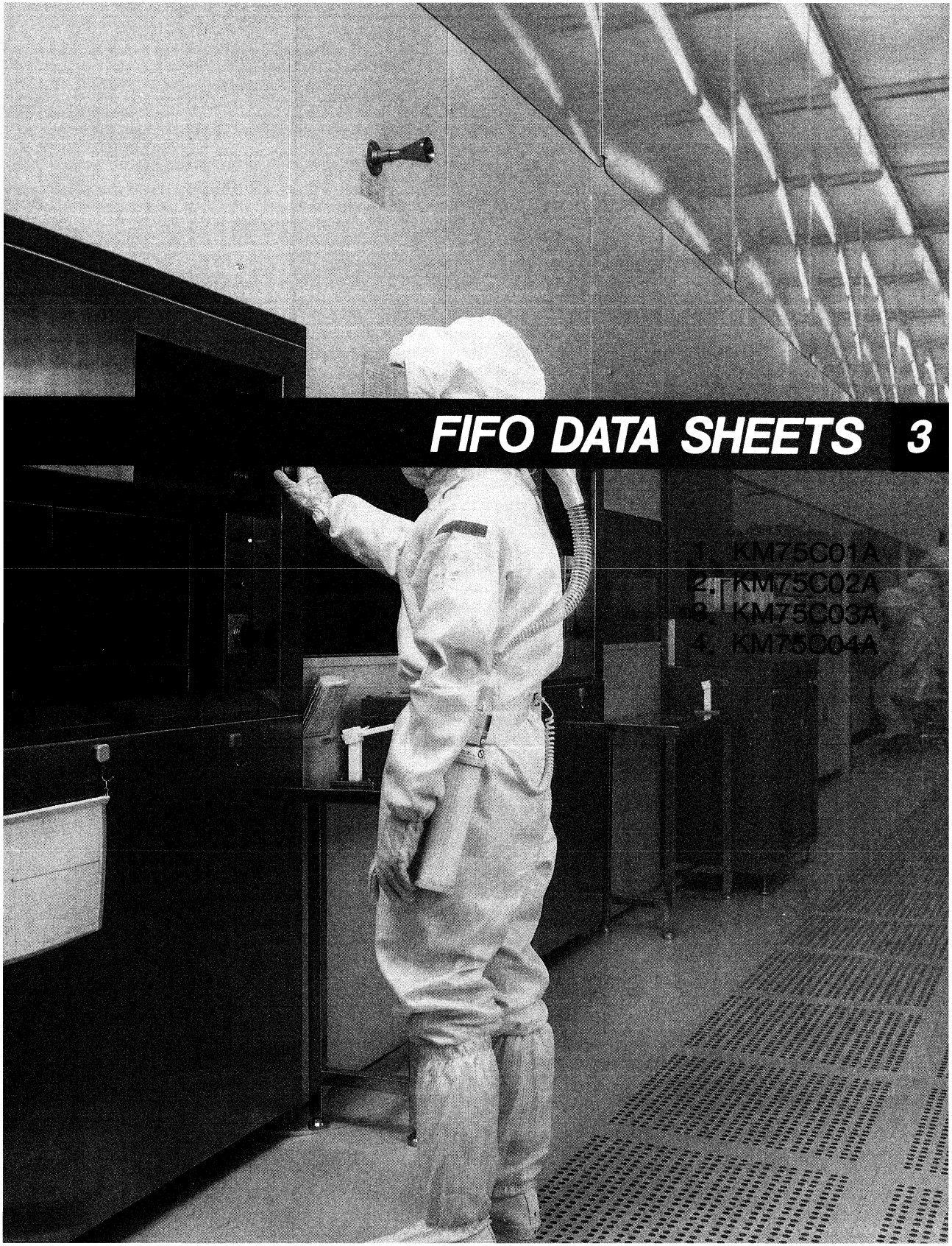


* 1 t_{AVCH}, t_{EVCH}, t_{GVCH}, t_{WVCH}
* 2 Valid data from CLK high is the data from the previous cycle
* 3 t_{EVCH}, t_{WVCH}, t_{GVCH}

PACKAGES DIMENSIONS

36 LEAD PLASTIC SMALL OUT LINE J FORM PACKAGE





FIFO DATA SHEETS 3

1. KM75C01A
2. KM75C02A
3. KM75C03A
4. KM75C04A

First-in First-out (FIFO) 512 x 9 CMOS Memory

FEATURES

- First-in, First-out dual port memory
  - 512 x 9 organization
- Very high speed independent of depth/width
  - 25ns cycle times
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or width
- Low power consumption
  - Active: 150mA (max)
  - Power Down: 15mA (max)
- KM75C01A pinout and functionality compatible with IDT IDT7201A and AMD Am 7201A
- Half-full flag capability in standalone mode
- Empty and full warning flags
- Auto retransmit capability in standalone mode
- High performance 1.2 micron CMOS technology
- Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC

DESCRIPTION

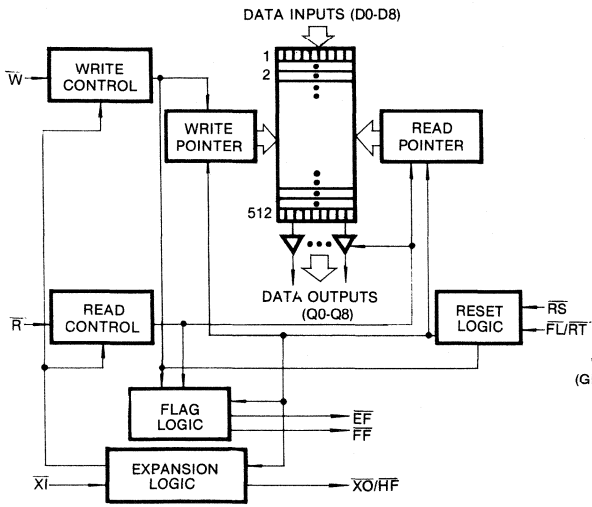
The KM75C01A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

No address information is required for KM75C01A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 25nsec (40MHz).

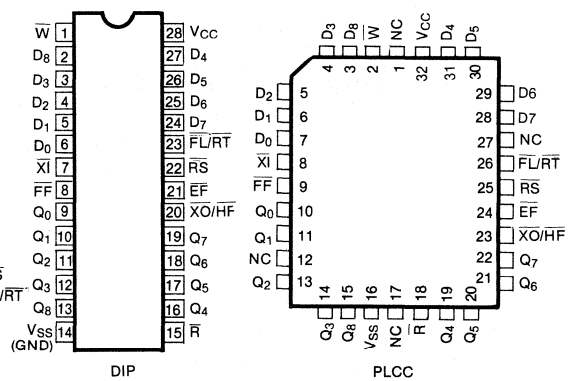
The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

The KM75C01A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_A	0 to +70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 15/20ns			T_A = 25ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			150			120	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4			2.4			V
Output Low Voltage Level ($I_{OL} = 8mA$)	V_{OL}			0.4			0.4	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 35ns			T_A = 50ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			100			60	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4			2.4			V
Output Low Voltage Level ($I_{OL} = 8mA$)	V_{OL}			0.4			0.4	V

Notes: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Measurements with $V_{SS} \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C01A-15		KM75C01A-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		30		ns
Access Time	t_A		15		20	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	15		20		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		15		15	ns
Write Cycle Time	t_{WC}	25		30		ns
Write Pulse Width[2]	t_{WPW}	15		20		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	10		12		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	25		30		ns
Reset Pulse Width[2]	t_{RS}	15		20		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	25		30		ns
Retransmit Pulse Width[2]	t_{RT}	15		20		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		25		30	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		25		30	ns
Read Low to Empty Flag High	t_{REF}		20		20	ns
Read High to Full Flag High	t_{RFF}		20		20	ns
Write High to Empty Flag High	t_{WEF}		20		20	ns
Write Low to Full Flag Low	t_{WFF}		20		20	ns
Write Low to Half-Full Flag Low	t_{WHF}		25		30	ns
Read High to Half-Full Flag High	t_{RHF}		25		30	ns
Expansion Out Low Delay from Clock	t_{XOL}		20		20	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		20		20	ns
$\overline{XI}$ Pulse Width	t_{PXI}	15		20		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	10		12		ns

3

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $+70°C$)

Parameter	Symbol	KM75C01A-25		KM75C01A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Access Time	t_A		25		35	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	25		35		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[1]	t_{RHZ}		20		20	ns
Write Cycle Time	t_{WC}	35		45		ns
Write Pulse Width[2]	t_{WPW}	25		35		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	15		18		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	35		45		ns
Reset Pulse Width[2]	t_{RS}	25		35		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	35		45		ns
Retransmit Pulse Width[2]	t_{RT}	25		35		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		35		45	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		35		45	ns
Read Low to Empty Flag High	t_{REF}		25		30	ns
Read High to Full Flag High	t_{RFF}		25		30	ns
Write High to Empty Flag High	t_{WEF}		25		30	ns
Write Low to Full Flag Low	t_{WFF}		25		30	ns
Write Low to Half-Full Flag Low	t_{WHF}		35		45	ns
Read High to Half-Full Flag High	t_{RHF}		35		45	ns
Expansion Out Low Delay from Clock	t_{XOL}		25		35	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		25		35	ns
$\overline{XI}$ Pulse Width	t_{PXI}	25		35		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C01A-50		KM75C01A-80		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	65		100		ns
Access Time	t_A		50		80	ns
Read Recovery Time	t_{RR}	15		20		ns
Read Pulse Width[2]	t_{RPW}	50		80		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		30		30	ns
Write Cycle Time	t_{WC}	65		100		ns
Write Pulse Width[2]	t_{WPW}	50		80		ns
Write Recovery Time	t_{WR}	15		20		ns
Data Setup Time	t_{DS}	30		40		ns
Data Hold Time	t_{DH}	5		10		ns
Reset Cycle Time	t_{RSC}	65		100		ns
Reset Pulse Width[2]	t_{RS}	50		80		ns
Reset Recovery Time	t_{RSR}	15		20		ns
Retransmit Cycle Time	t_{RTC}	65		100		ns
Retransmit Pulse Width[2]	t_{RT}	50		80		ns
Retransmit Recovery Time	t_{RTR}	15		20		ns
Reset to Empty Flag Low	t_{EFL}		65		100	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		65		100	ns
Read Low to Empty Flag High	t_{REF}		45		60	ns
Read High to Full Flag High	t_{RFF}		45		60	ns
Write High to Empty Flag High	t_{WEF}		45		60	ns
Write Low to Full Flag Low	t_{WFF}		45		60	ns
Write Low to Half-Full Flag Low	t_{WHF}		65		100	ns
Read High to Half-Full Flag High	t_{RHF}		65		100	ns
Expansion Out Low Delay from Clock	t_{XOL}		50		80	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		50		65	ns
$\overline{XI}$ Pulse Width	t_{PXI}	50		80		ns
$\overline{XI}$ Recovery Time	t_{XIR}	15		20		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

Notes: 1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

AC TEST CONDITIONS

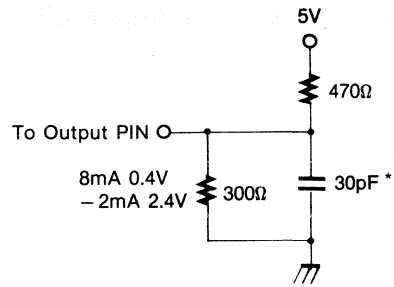
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note: This parameter is sampled and not 100% tested.

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

Note: Generation $\overline{R}/\overline{W}$ Signals-When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

Master Reset ($\overline{RS}$)

Reset is accomplished whenever the MASTER RESET ($\overline{RS}$) input is taken to a low state. During this operation, both the internal read and the internal write pointers are set to the first FIFO location. A Master Reset pulse is required to initialize the FIFO after power-up before any write operation is performed. Both $\overline{R}$ and $\overline{W}$ inputs must be inactive for t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change for t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be set to inactive (high) level after master reset ($\overline{RS}$).

Read Enable ($\overline{R}$)

READ cycles are initiated on the falling edge of the READ ENABLE ($\overline{R}$) input provided that EMPTY-FLAG ($\overline{EF}$) is not low. Read Cycles may be initiated asynchronously to any write operation in progress. After READ ENABLE ($\overline{R}$) goes high, the data outputs will return to a high impedance condition until the next READ operation. If the FIFO is empty, the EMPTY-FLAG ($\overline{EF}$) will go low and prevent any further read cycles. The data outputs will enter the high-impedance state after completion of the last read cycle.

Write Enable ($\overline{W}$)

WRITE cycles may be initiated by a low signal at the $\overline{W}$ input provided the FULL-FLAG ($\overline{FF}$) is not set. Data is stored in the memory array sequentially independent of any read operation that may be in progress.

When more than half of the memory bytes have been filled, the HALF-FULL ($\overline{HF}$) Flag output will be set low and will remain low till the difference between the write pointer and read pointer is less than or equal to one half of the total memory bytes of the device. The HALF-FULL flag is then reset by the rising edge of the read operation.

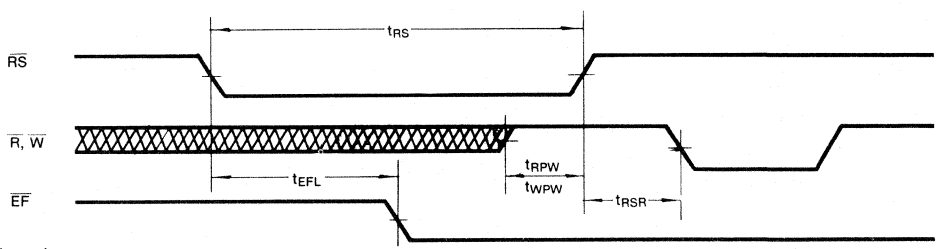
When the memory array is completely full, i.e., when the write pointer is one location from the read pointer, the FULL-FLAG ($\overline{FF}$) will go low preventing any further write operations. The FULL-FLAG will go high again t_{RFF} after completion of a valid read operation.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This input may be used in two different ways depending upon the configuration of EXPANSION-IN ($\overline{XI}$):

1. Single Device or Retransmit Mode: In this mode the $\overline{XI}$ pin must be grounded. Using this mode the device can be used to retransmit data when $\overline{RT}$ is pulsed low. A retransmit operation will set the internal read pointer

Figure 2. Reset



Notes

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{RS}$.

to the first memory location in the array. The write pointer is unaffected. Both write enable and read enable must be inactive during the retransmit operation. This feature is particularly useful for FIFO applications in communications buffers where noise levels may be high and transmission errors are frequently detected. The retransmit feature may not be used along with depth expansion.

2. Depth Expansion Mode: In this mode the ($\overline{FL}/\overline{RT}$) pin is grounded it that device is the first of the "daisy chain." The $\overline{FL}$ pin is kept high if it is further down the chain. For details of Depth Expansion see Operating Modes.

Expansion-In ($\overline{XI}$)

This is a dual purpose input pin. As explained above, $\overline{XI}$ is grounded to indicate single device mode operation. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain" in the Depth Expansion mode.

Full-Flag ($\overline{FF}$)

The FULL-FLAG output goes low inhibiting further write operations when the write pointer is one memory location from the read pointer i.e., the memory array is full. The total length of the memory array is 512 bytes write operations for the KM75C01A.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This output may be used in two different ways:

Single Device Mode: In this mode this output acts as a HALF-FULL Flag. After half the memory locations are full, and at the falling edge of the next write operation, the $\overline{HF}$ output is set to low. It is reset to high if the difference between the write pointer and the read pointer is half the memory depth or less at the rising edge of the read operation.

Depth Expansion Mode: In this mode EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain." In this way a signal can be passed onto the next device when the current device reaches the last memory location.

FIFO's can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$'s together. $\overline{HF}$ and $\overline{RT}$ functions are available in Depth Expansion Mode.

Single Device/Width Expansion Mode: Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a MR cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFO's can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Figure 3. Asynchronous Write and Read Operation

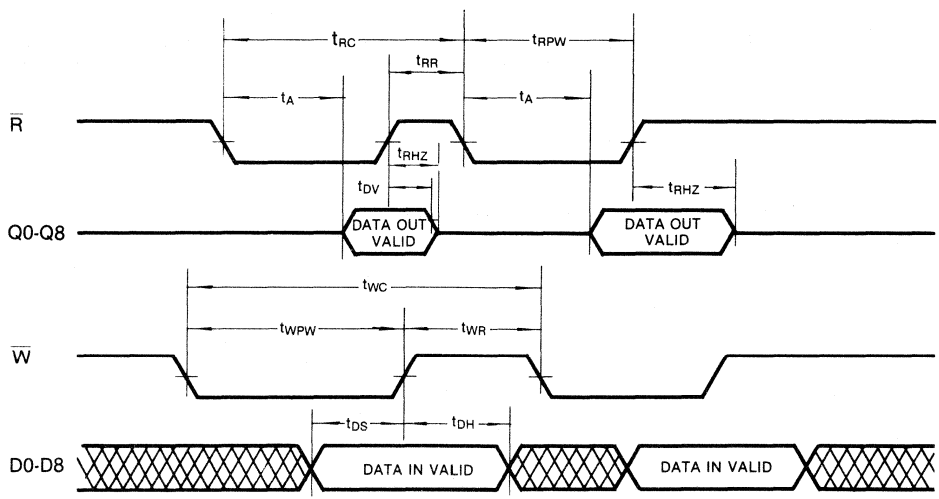


Figure 4. Full Flag From Last Write to First Read

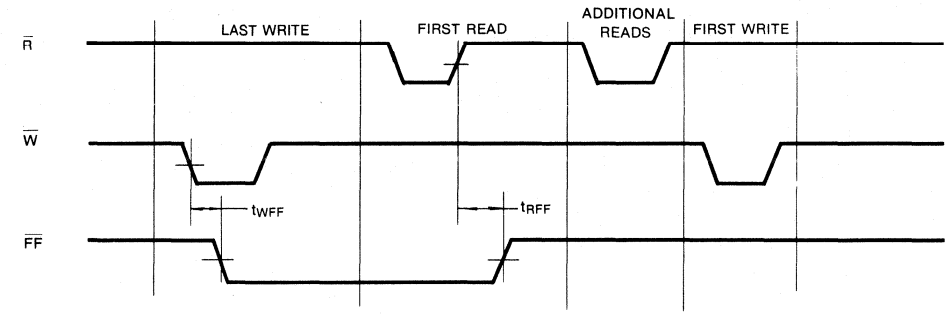


Figure 5. Empty Flag From Last Read to First Write

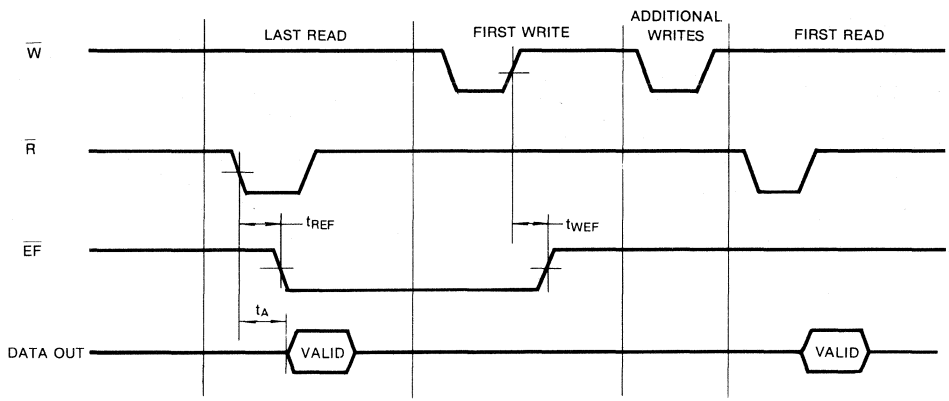
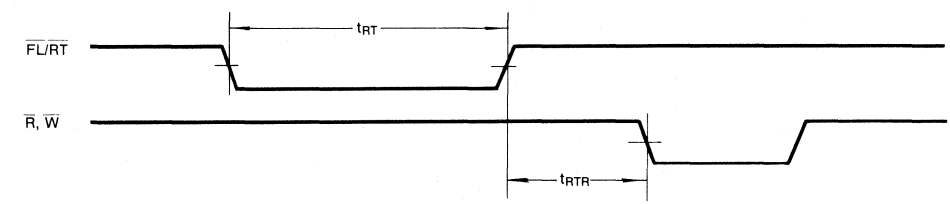


Figure 6. Retransmit



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Expansion-In Timing Diagram

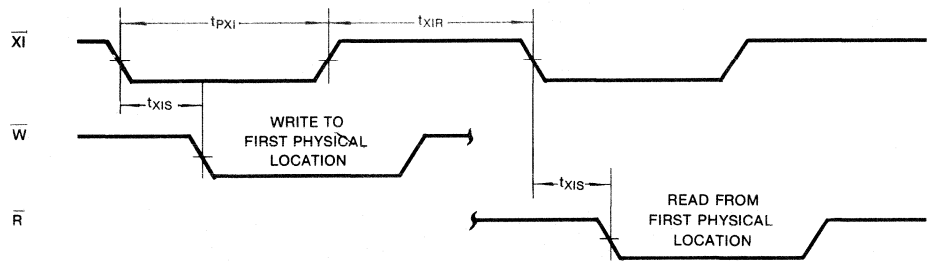


Figure 8. Expansion-Out Timing Diagram

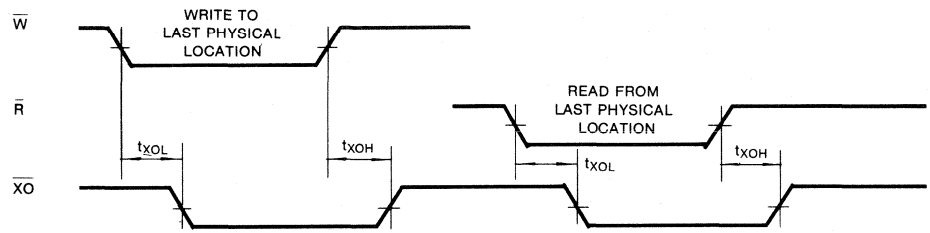
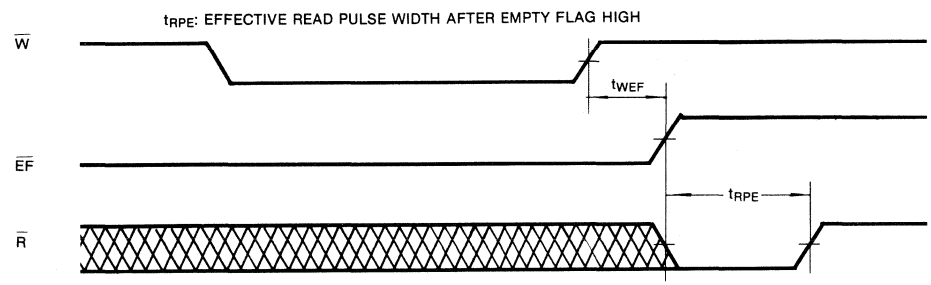


Figure 9. Empty Flag Timing



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 10. Full Flag Timing

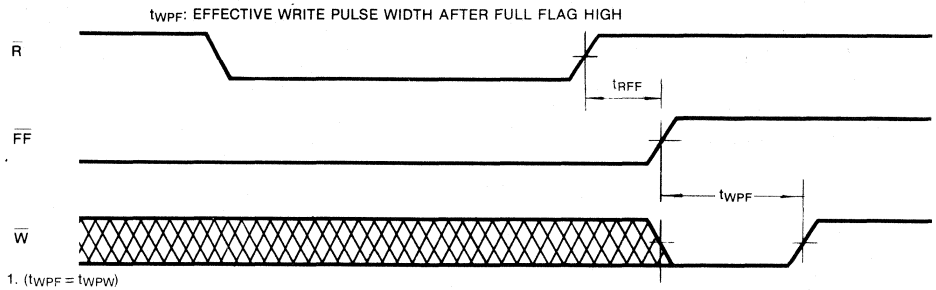
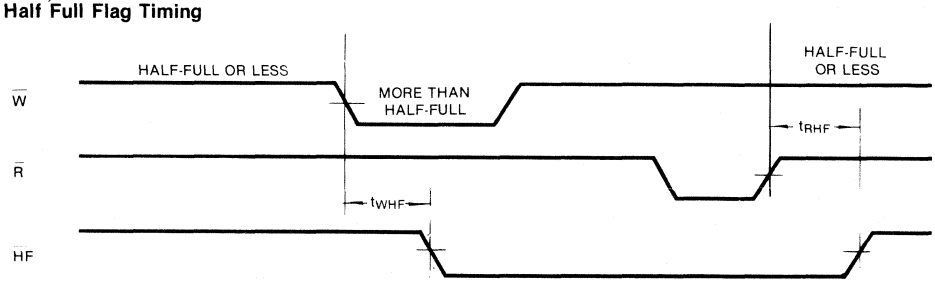


Figure 11. Half Full Flag Timing



OPERATING MODES

Single Device Mode

A single KM75C01A may be used when the application requirements are for 512 words or less, the device is placed in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded (See Figure 12). In this mode the HALF-FULL FLAG ($\overline{HF}$) and RETRANSMIT ($\overline{RT}$) features are available.

Figure 12. Block Diagram of Single 512 × 9 FIFO

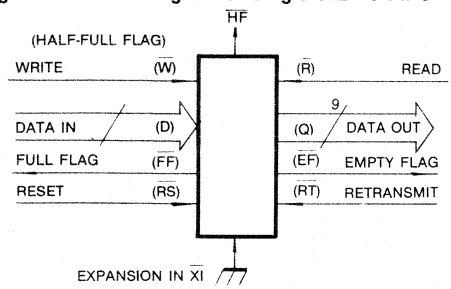
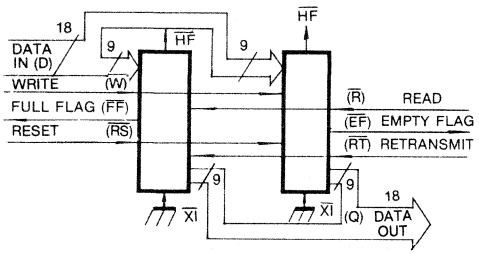


Figure 13. Block Diagram of 512 × 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Width Expansion Mode

Word width may be increased simply by connecting he corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two KM75C01A. Any word width can be attained by adding additional KM75C01A.

Depth Expansion (Daisy Chain) Mode

The KM75C01A can easily be adapted to applications when the requirements are for greater than 512 words. Figure 14 demonstrates Depth Expansion using three KM75C01A. Any depth can be attained by adding additional KM75C01A. The KM75C01A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input. The RETRANSMIT feature is not available in this mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. The half-full flag ($\overline{HF}$) function is not available in this mode.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (See Figure 15).

Bidirectional Mode

Applications which required data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing KM75C01A as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

This section describes two special conditions—when the FIFO is full or empty. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a tri-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the emptly flag); however, the same word (written the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data (from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

TRUTH TABLES

Table 1. Reset and Retransmit-Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1. Pointer will increment if flag is high

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$
Reset	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

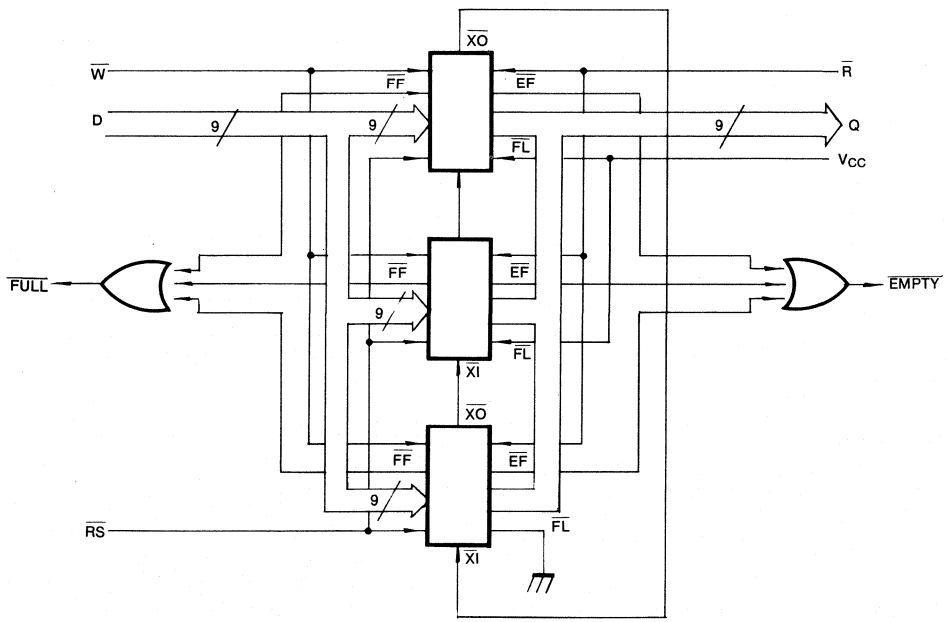


Figure 15. Compound FIFO Expansion

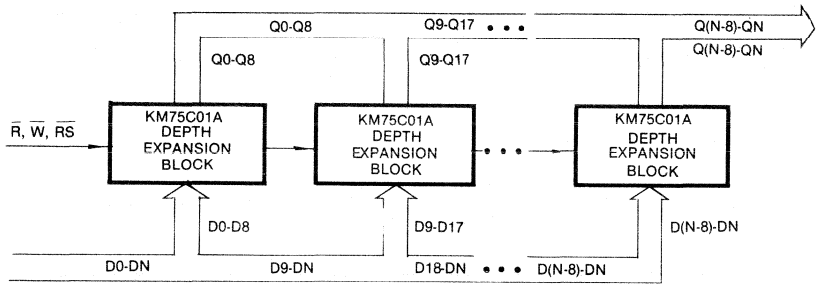
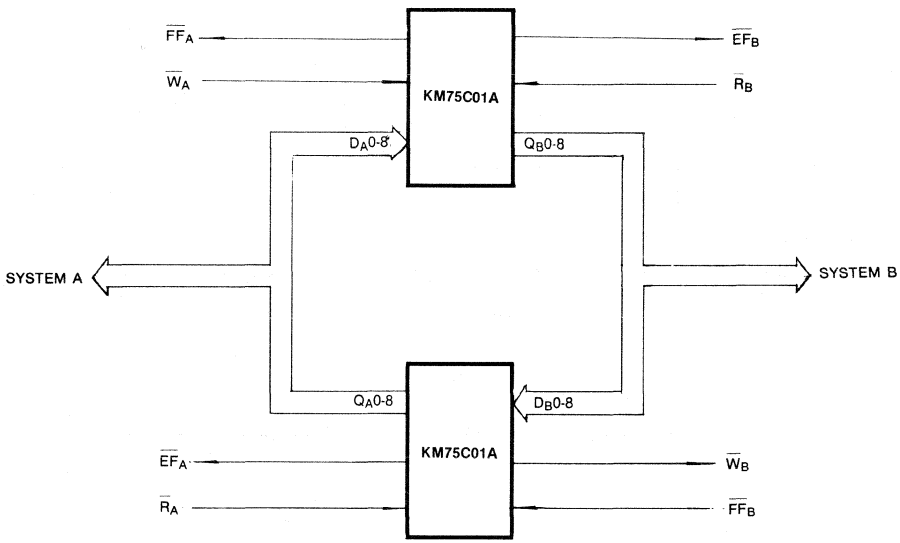
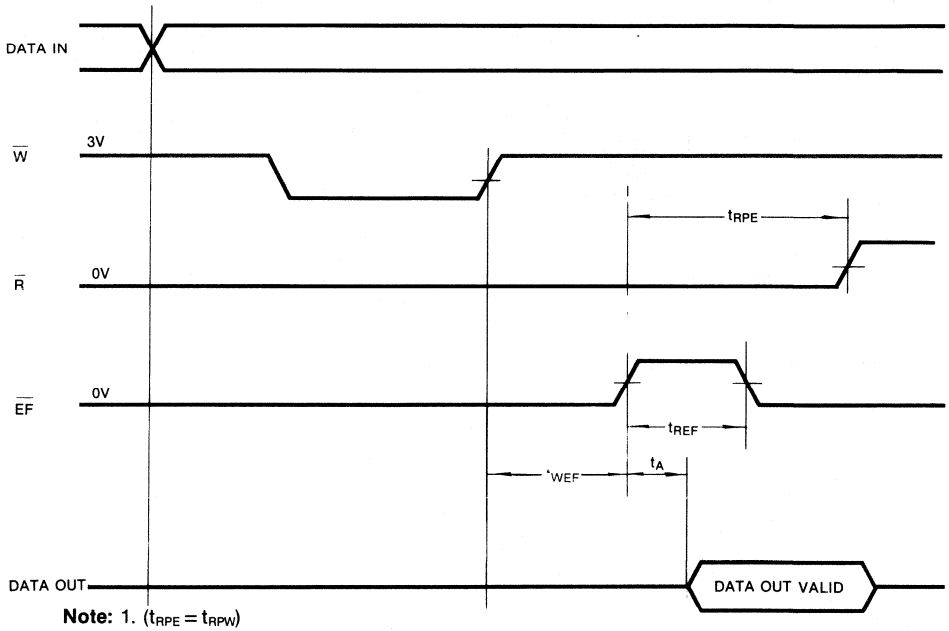


Figure 16. Bidirectional FIFO Mode



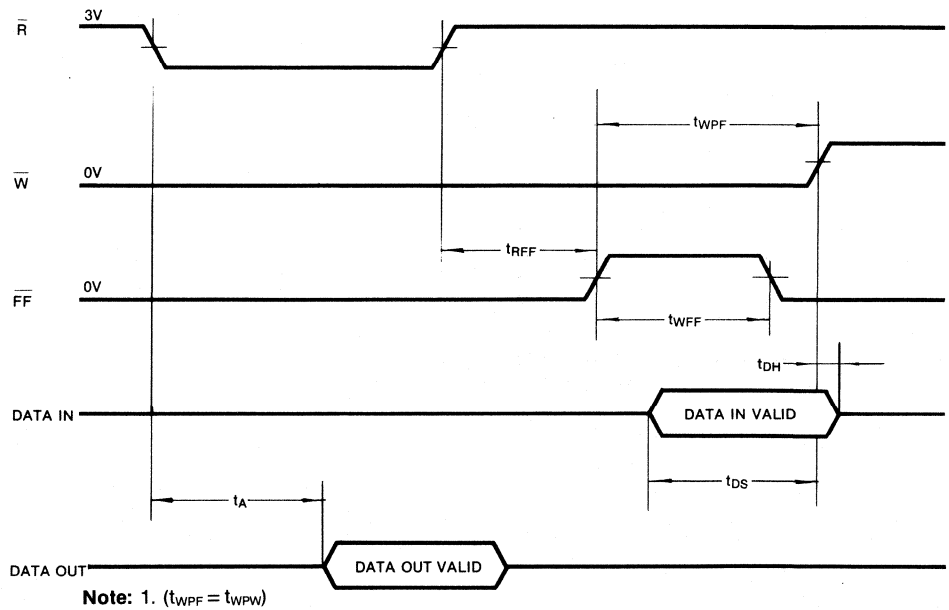
Notes:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 14.
2. For detection see WIDTH EXPANSION Section and Figure 13.

Figure 17. Read Data Flow Through Mode



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 18. Write Data Flow Through Mode

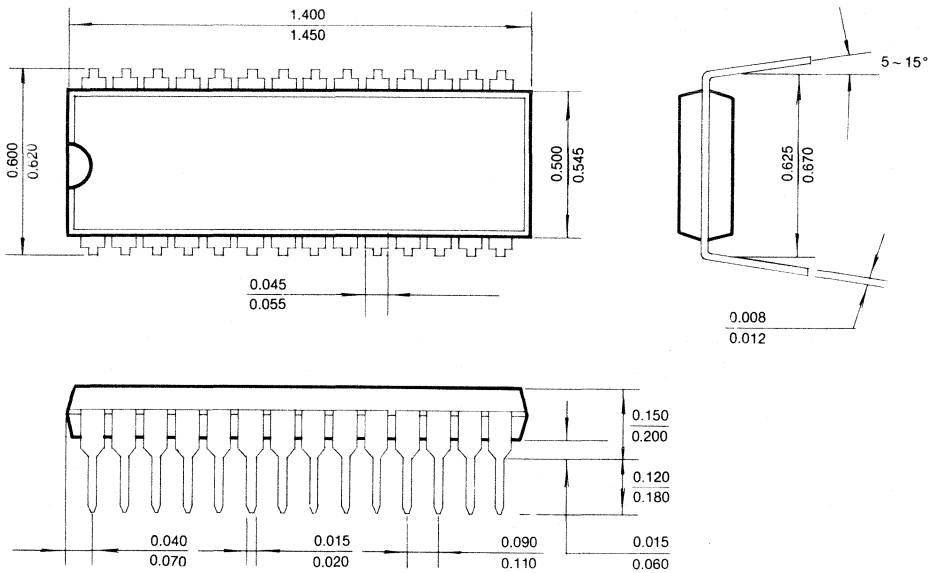


Note: 1. ($t_{WPF} = t_{WPW}$)

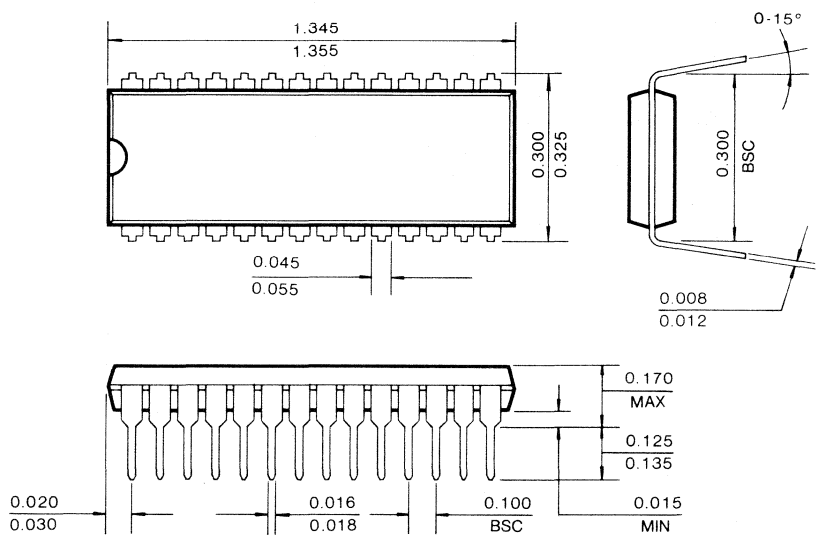
PACKAGE DIMENSIONS

28 PIN PLASTIC DIP (600mil)

Unit (inches)



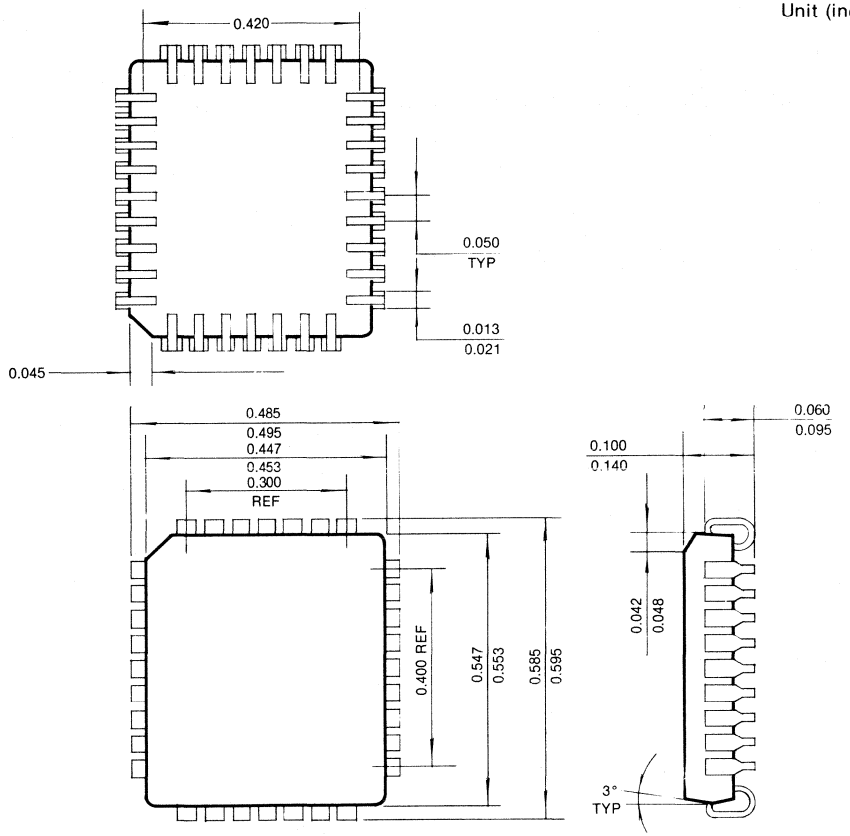
28 PIN PLASTIC DIP (300mil)



PACKAGE DIMENSIONS (Continued)

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

Unit (inches)



First-in First-out (FIFO) 1024 x 9 CMOS Memory

FEATURES

- First-in, First-out dual port memory
  - 1024 x 9 organization
- Very high speed independent of depth/width
  - 20ns cycle times
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or width
- Low power consumption
  - Active: 150mA (max)
  - Power Down: 15mA (max)
- KM75C02A allows for deep word structure (1024) without expansion-pin and functionally compatible with AMD Am7202 and IDT7202A
- Half-full flag capability in standalone mode
- Empty and full warning flags
- Auto retransmit capability in standalone mode
- High performance 1.2 micron CMOS technology
- Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC

DESCRIPTION

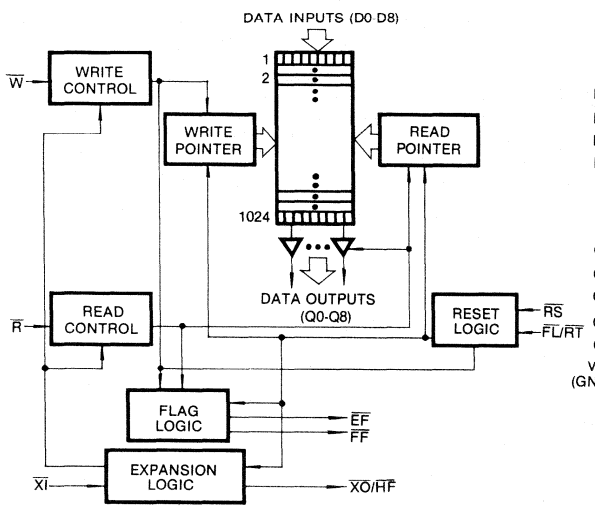
The KM75C02A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

No address information is required for KM75C02A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 20nsec (50MHz).

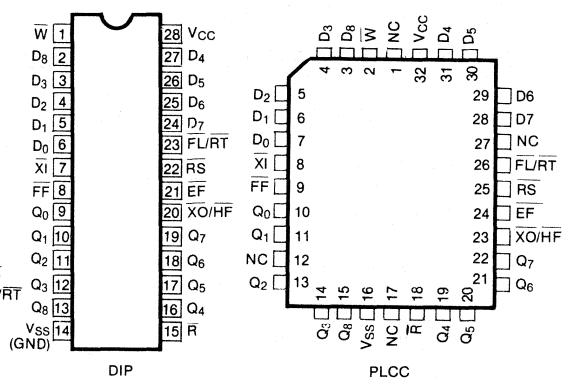
The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

The KM75C02A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_A	0 to +70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 15/20ns			T_A = 25ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			150			120	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4			2.4			V
Output Low Voltage Level ($I_{OL} = 8mA$)	V_{OL}			0.4			0.4	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 35ns			T_A = 50ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			100			60	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4			2.4			V
Output Low Voltage Level ($I_{OL} = 8mA$)	V_{OL}			0.4			0.4	V

Notes: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Measurements with $V_{SS} \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to + 70°C)

Parameter	Symbol	KM75C02A-12		KM75C02A-15		KM75C02A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		30		ns
Access Time	t_A		12		15		20	ns
Read Recovery Time	t_{RR}	8		10		10		ns
Read Pulse Width(2)	t_{RPW}	12		15		20		ns
Data Valid from Read Pulse High	t_{DV}	5		5		5		ns
Read Pulse High to Data Bus at High-Z(3)	t_{RHZ}		15		15		15	ns
Write Cycle Time	t_{WC}	20		25		30		ns
Write Pulse Width(2)	t_{WPW}	12		15		20		ns
Write Recovery Time	t_{WR}	8		10		10		ns
Data Setup Time	t_{DS}	8		10		12		ns
Data Hold Time	t_{DH}	0		0		0		ns
Reset Cycle Time	t_{RSC}	20		25		30		ns
Reset Pulse Width(2)	t_{RS}	12		15		20		ns
Reset Recovery Time	t_{RSR}	8		10		10		ns
Retransmit Cycle Time	t_{RTC}	25		25		30		ns
Retransmit Pulse Width(2)	t_{RT}	15		15		20		ns
Retransmit Recovery Time	t_{RTR}	10		10		10		ns
Reset to Empty Flag Low	t_{EFL}		20		25		30	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		20		25		30	ns
Read Low to Empty Flag High	t_{REF}		20		20		20	ns
Read High to Full Flag High	t_{RFF}		20		20		20	ns
Write High to Empty Flag High	t_{WEF}		20		20		20	ns
Write Low to Full Flag Low	t_{WFF}		20		20		20	ns
Write Low to Half-Full Flag Low	t_{WHF}				25		30	ns
Read High to Half-Full Flag High	t_{RHF}				25		30	ns
Expansion Out Low Delay from Clock	t_{XOL}		16		20		20	ns
Expansion Out High Delay from Clock	t_{XOH}(4)		16		20		20	ns
$\overline{XI}$ Pulse Width	t_{PXI}	12		15		20		ns
$\overline{XI}$ Recovery Time	t_{XIR}	8		10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	8		10		12		ns

3

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C02A-25		KM75C02A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Access Time	t_A		25		35	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	25		35		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[1]	t_{RHZ}		20		20	ns
Write Cycle Time	t_{WC}	35		45		ns
Write Pulse Width[2]	t_{WPW}	25		35		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	15		18		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	35		45		ns
Reset Pulse Width[2]	t_{RS}	25		35		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	35		45		ns
Retransmit Pulse Width[2]	t_{RT}	25		35		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		35		45	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		35		45	ns
Read Low to Empty Flag High	t_{REF}		25		30	ns
Read High to Full Flag High	t_{RFF}		25		30	ns
Write High to Empty Flag High	t_{WEF}		25		30	ns
Write Low to Full Flag Low	t_{WFF}		25		30	ns
Write Low to Half-Full Flag Low	t_{WHF}		35		45	ns
Read High to Half-Full Flag High	t_{RHF}		35		45	ns
Expansion Out Low Delay from Clock	t_{XOL}		25		35	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		25		35	ns
$\overline{XI}$ Pulse Width	t_{PXI}	25		35		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

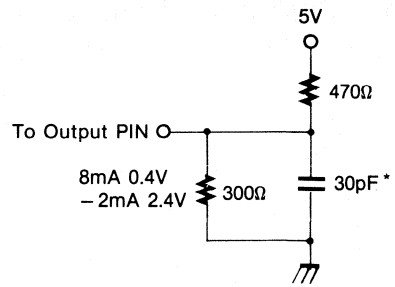
Parameter	Symbol	KM75C02A-50		KM75C02A-80		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	65		100		ns
Access Time	t_A		50		80	ns
Read Recovery Time	t_{RR}	15		20		ns
Read Pulse Width[2]	t_{RPW}	50		80		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		30		30	ns
Write Cycle Time	t_{WC}	65		100		ns
Write Pulse Width[2]	t_{WPW}	50		80		ns
Write Recovery Time	t_{WR}	15		20		ns
Data Setup Time	t_{DS}	30		40		ns
Data Hold Time	t_{DH}	5		10		ns
Reset Cycle Time	t_{RSC}	65		100		ns
Reset Pulse Width[2]	t_{RS}	50		80		ns
Reset Recovery Time	t_{RSR}	15		20		ns
Retransmit Cycle Time	t_{RTC}	65		100		ns
Retransmit Pulse Width[2]	t_{RT}	50		80		ns
Retransmit Recovery Time	t_{RTR}	15		20		ns
Reset to Empty Flag Low	t_{EFL}		65		100	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		65		100	ns
Read Low to Empty Flag High	t_{REF}		45		60	ns
Read High to Full Flag High	t_{RFF}		45		60	ns
Write High to Empty Flag High	t_{WEF}		45		60	ns
Write Low to Full Flag Low	t_{WFF}		45		60	ns
Write Low to Half-Full Flag Low	t_{WHF}		65		100	ns
Read High to Half-Full Flag High	t_{RHF}		65		100	ns
Expansion Out Low Delay from Clock	t_{XOL}		50		80	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		50		65	ns
$\overline{XI}$ Pulse Width	t_{PXI}	50		80		ns
$\overline{XI}$ Recovery Time	t_{XIR}	15		20		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

Notes: 1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note: This parameter is sampled and not 100% tested.

Note: Generation $\overline{R}/\overline{W}$ Signals-When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

Master Reset ($\overline{RS}$)

Reset is accomplished whenever the MASTER RESET ($\overline{RS}$) input is taken to a low state. During this operation, both the internal read and the internal write pointers are set to the first FIFO location. A Master Reset pulse is required to initialize the FIFO after power-up before any write operation is performed. Both $\overline{R}$ and $\overline{W}$ inputs must be inactive for t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change for t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be set to inactive (high) level after master reset ($\overline{RS}$).

Read Enable ($\overline{R}$)

READ cycles are initiated on the falling edge of the READ ENABLE ($\overline{R}$) input provided that EMPTY-FLAG ($\overline{EF}$) is not low. Read Cycles may be initiated asynchronously to any write operation in progress. After READ ENABLE ($\overline{R}$) goes high, the data outputs will return to a high impedance condition until the next READ operation. If the FIFO is empty, the EMPTY-FLAG ($\overline{EF}$) will go low and prevent any further read cycles. The data outputs will enter the high-impedance state after completion of the last read cycle.

Write Enable ($\overline{W}$)

WRITE cycles may be initiated by a low signal at the $\overline{W}$ input provided the FULL-FLAG ($\overline{FF}$) is not set. Data is stored in the memory array sequentially independent of any read operation that may be in progress.

When more than half of the memory bytes have been filled, the HALF-FULL ($\overline{HF}$) Flag output will be set low and will remain low till the difference between the write pointer and read pointer is less than or equal to one half of the total memory bytes of the device. The HALF-FULL flag is then reset by the rising edge of the read operation.

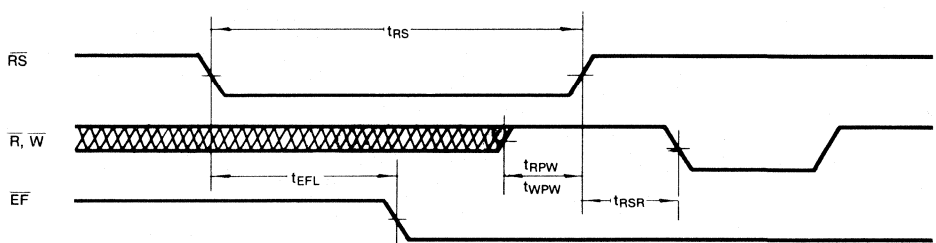
When the memory array is completely full, i.e., when the write pointer is one location from the read pointer, the FULL-FLAG ($\overline{FF}$) will go low preventing any further write operations. The FULL-FLAG will go high again t_{RFF} after completion of a valid read operation.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This input may be used in two different ways depending upon the configuration of EXPANSION-IN ($\overline{XI}$):

1. Single Device or Retransmit Mode: In this mode the $\overline{XI}$ pin must be grounded. Using this mode the device can be used to retransmit data when $\overline{RT}$ is pulsed low. A retransmit operation will set the internal read pointer

Figure 2. Reset



Notes

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{RS}$.

to the first memory location in the array. The write pointer is unaffected. Both write enable and read enable must be inactive during the retransmit operation. This feature is particularly useful for FIFO applications in communications buffers where noise levels may be high and transmission errors are frequently detected. The retransmit feature may not be used along with depth expansion.

2. Depth Expansion Mode: In this mode the ($\overline{FL}/\overline{RT}$) pin is grounded it that device is the first of the "daisy chain." The $\overline{FL}$ pin is kept high if it is further down the chain. For details of Depth Expansion see Operating Modes.

Expansion-In ($\overline{XI}$)

This is a dual purpose input pin. As explained above, $\overline{XI}$ is grounded to indicate single device mode operation. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain" in the Depth Expansion mode.

Full-Flag ($\overline{FF}$)

The FULL-FLAG output goes low inhibiting further write operations when the write pointer is one memory location from the read pointer i.e. the memory array is full. The total length of the memory array is 1024 bytes write operations for the KM75C02A.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This output may be used in two different ways:

Single Device Mode: In this mode this output acts as a HALF-FULL Flag. After half the memory locations are full, and at the falling edge of the next write operation, the $\overline{HF}$ output is set to low. It is reset to high if the difference between the write pointer and the read pointer is half the memory depth or less at the rising edge of the read operation.

Depth Expansion Mode: In this mode EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain." In this way a signal can be passed onto the next device when the current device reaches the last memory location.

FIFO's can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$'s together. $\overline{HF}$ and $\overline{RT}$ functions are available in Depth Expansion Mode.

Single Device/Width Expansion Mode: Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a MR cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFO's can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Figure 3. Asynchronous Write and Read Operation

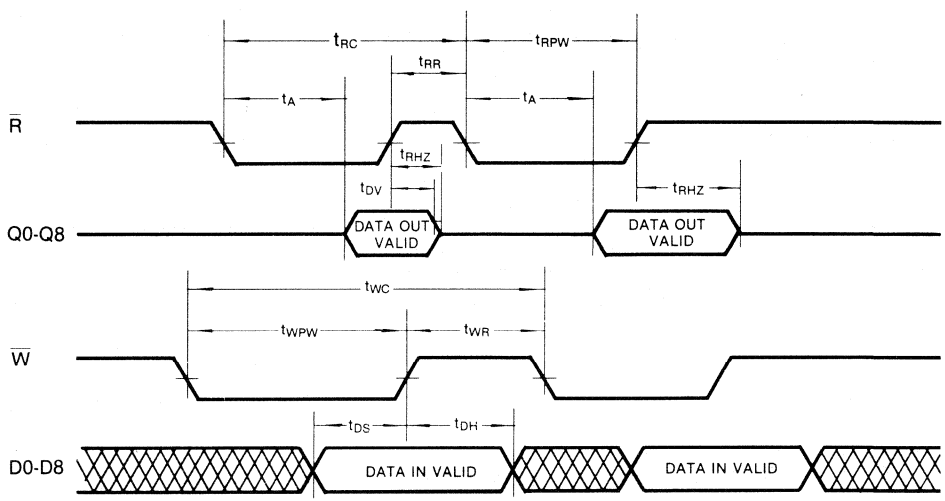


Figure 4. Full Flag From Last Write to First Read

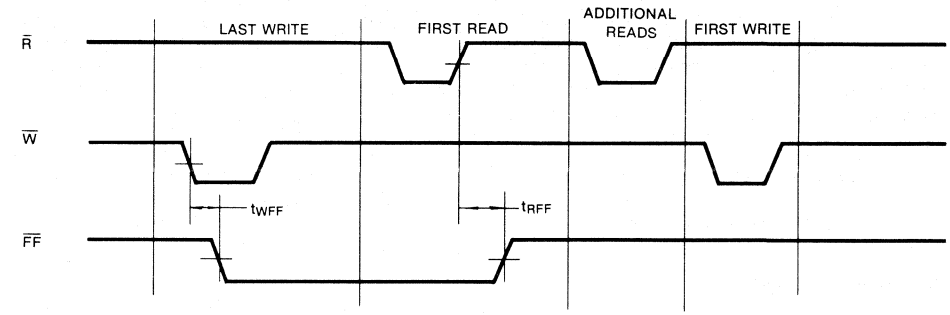


Figure 5. Empty Flag From Last Read to First Write

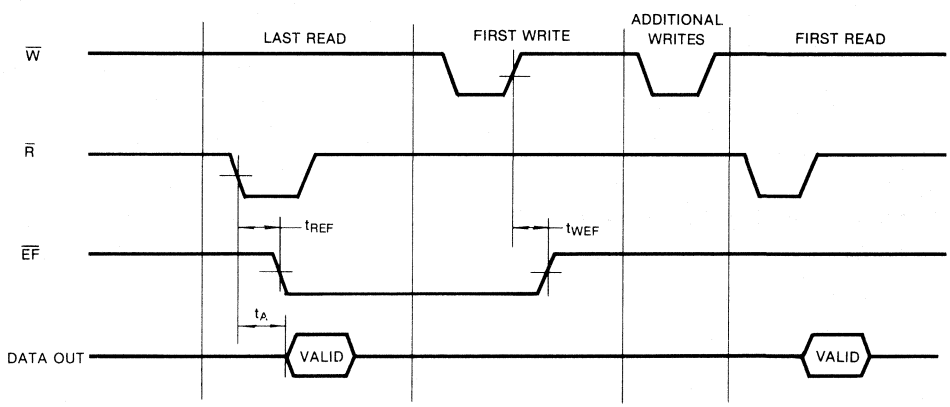
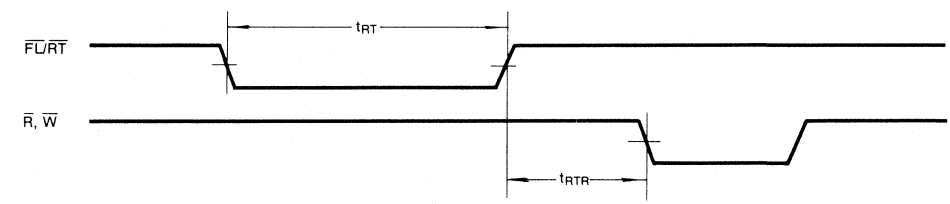


Figure 6. Retransmit



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Expansion-In Timing Diagram

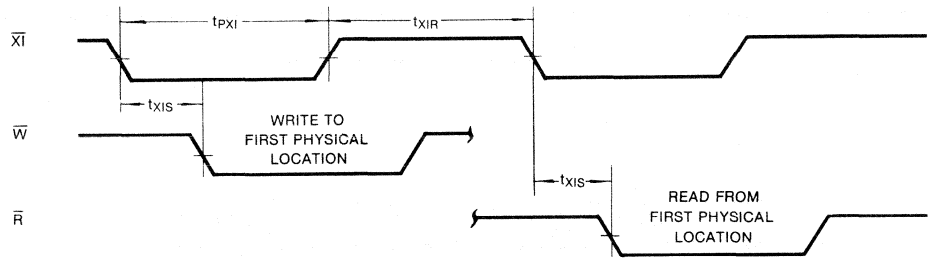


Figure 8. Expansion-Out Timing Diagram

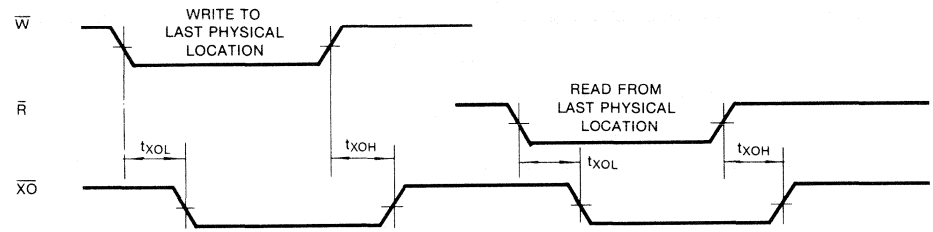
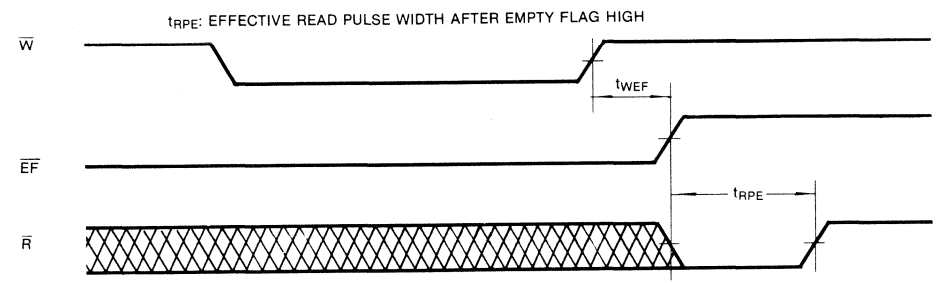


Figure 9. Empty Flag Timing



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 10. Full Flag Timing

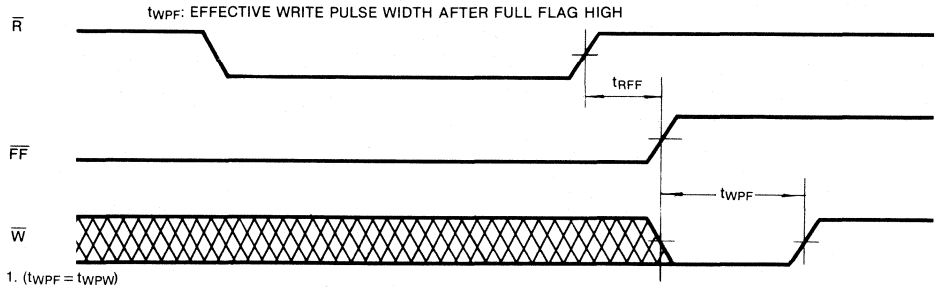
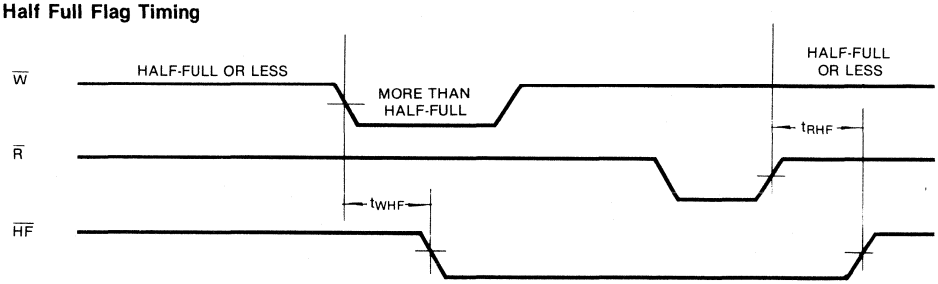


Figure 11. Half Full Flag Timing



OPERATING MODES

Single Device Mode

A single KM75C02A may be used when the application requirements are for 1024 words or less, the device is placed in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded (See Figure 12). In this mode the HALF-FULL FLAG ($\overline{HF}$) and RETRANSMIT ($\overline{RT}$) features are available.

Figure 12. Block Diagram of Single 1024 x 9 FIFO

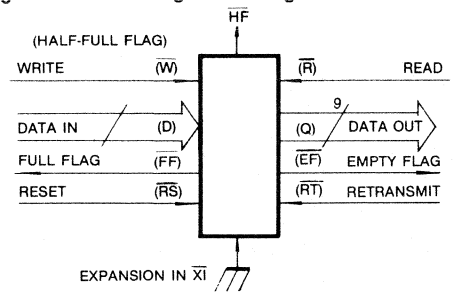
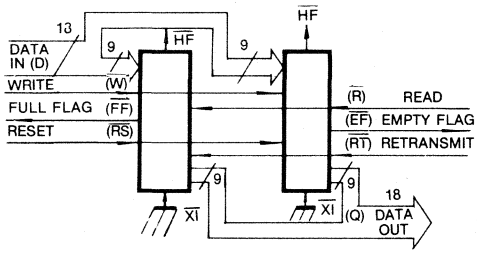


Figure 13. Block Diagram of 1024 x 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Width Expansion Mode

Word width may be increased simply by connecting he corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two KM75C02A. Any word width can be attained by adding additional KM75C02A.

Depth Expansion (Daisy Chain) Mode

The KM75C02A can easily be adapted to applications when the requirements are for greater than 1024 words. Figure 14 demonstrates Depth Expansion using three KM75C02A. Any depth can be attained by adding additional KM75C02A. The KM75C02A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input. The RETRANSMIT feature is not available in this mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. The half-full flag ($\overline{HF}$) function is not available in this mode.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (See Figure 15).

Bidirectional Mode

Applications which required data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing KM75C02A as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

This sect taken to bes two special conditions—when the FIFO is full or empty. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a tri-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the emptly flag); however, the same word (written the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data (from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

TRUTH TABLES

Table 1. Reset and Retransmit-Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1. Pointer will increment if flag is high

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$
Reset	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output,
$\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

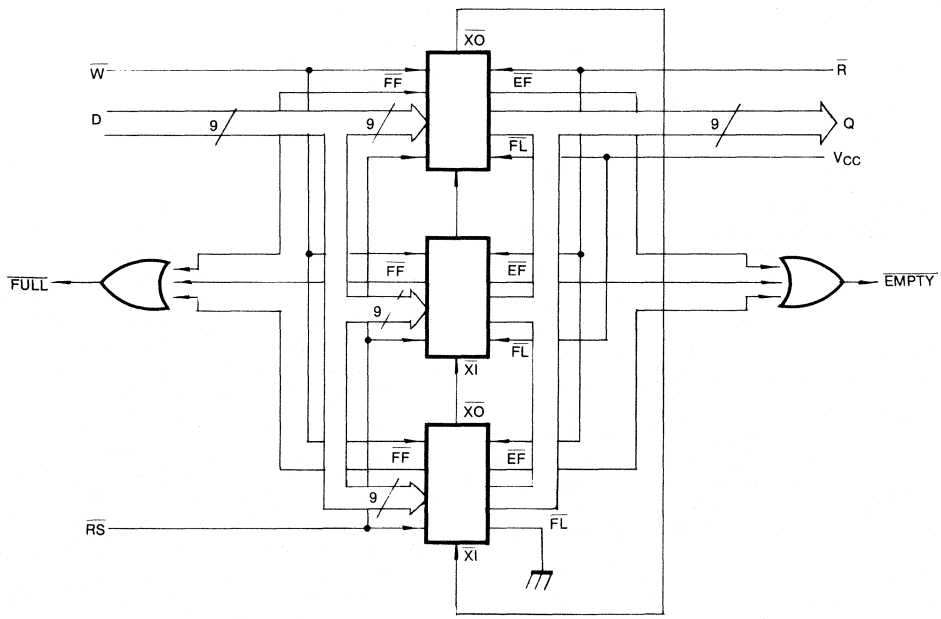


Figure 15. Compound FIFO Expansion

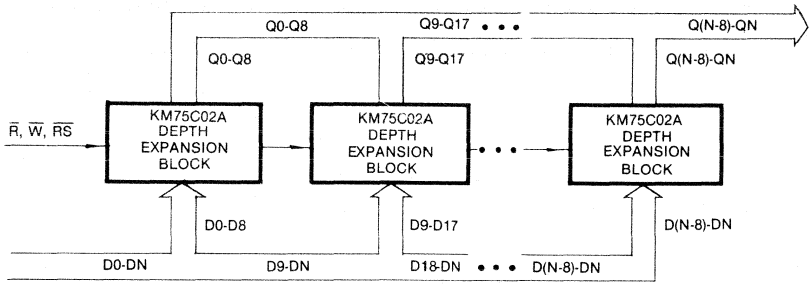
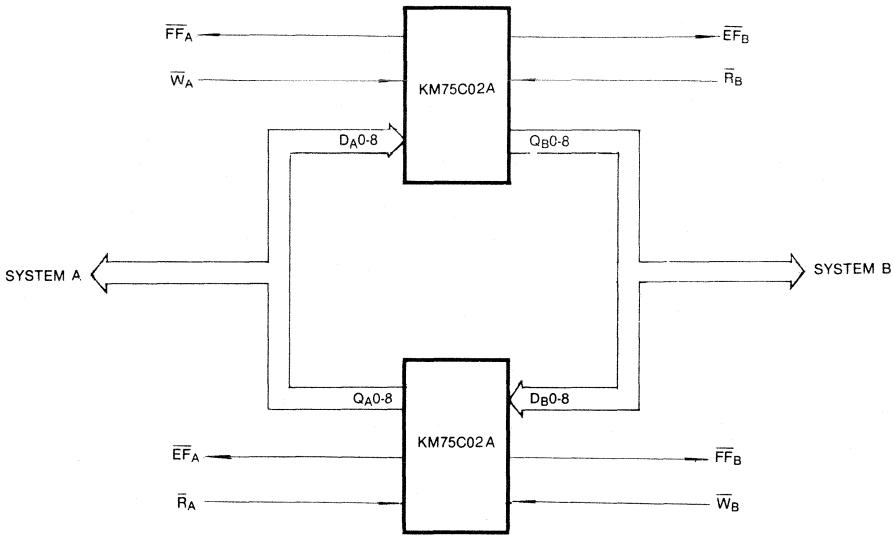
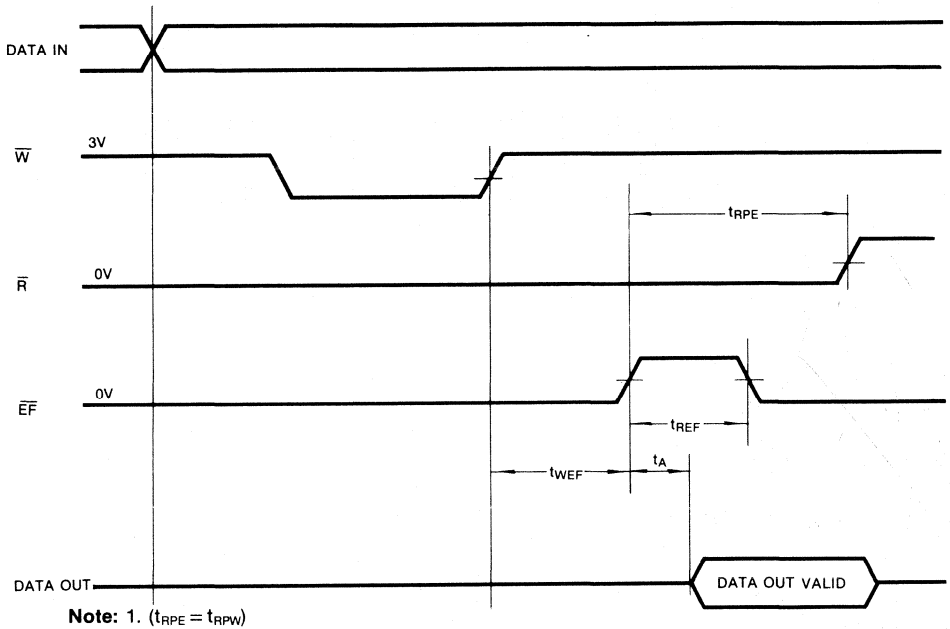


Figure 16. Bidirectional FIFO Mode



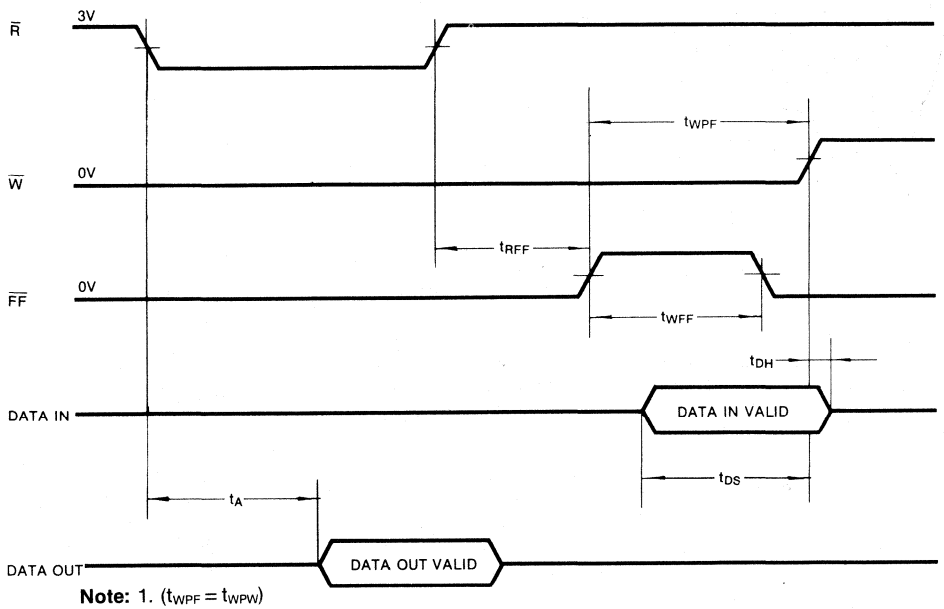
Notes:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 14.
2. For detection see WIDTH EXPANSION Section and Figure 13.

Figure 17. Read Data Flow Through Mode



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 18. Write Data Flow Through Mode

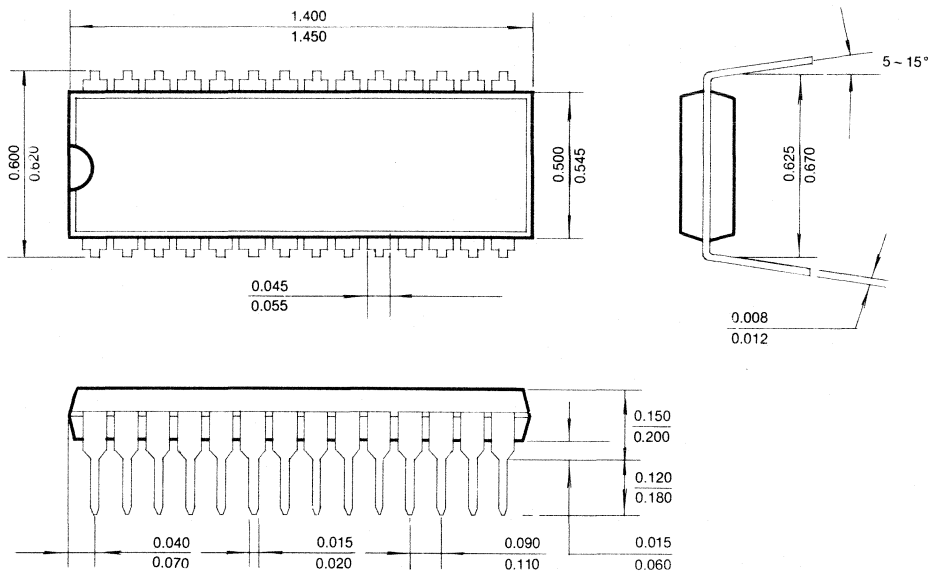


Note: 1. ($t_{WPF} = t_{WPW}$)

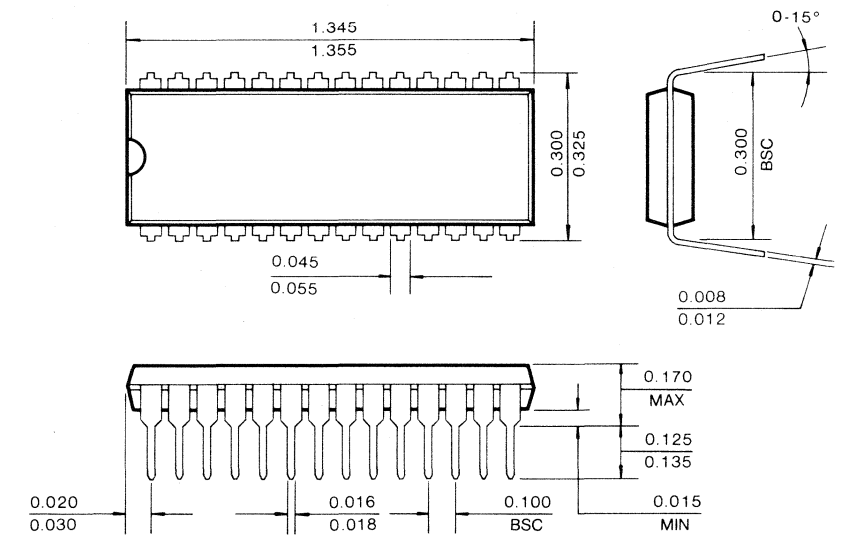
PACKAGE DIMENSIONS

28 PIN PLASTIC DIP (600mil)

Unit (inches)



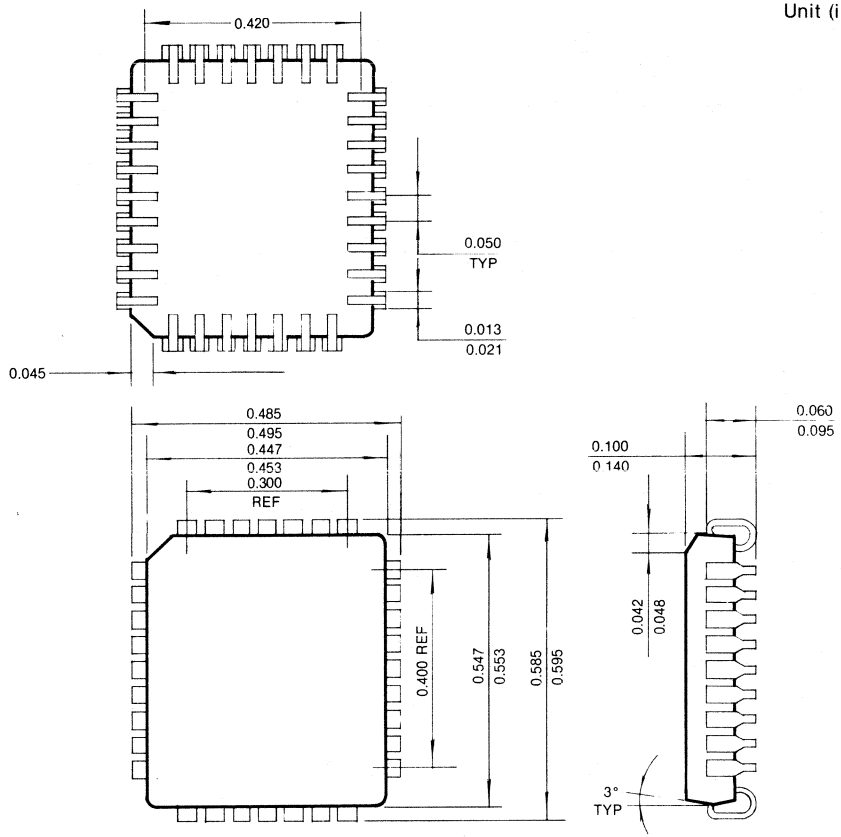
28 PIN PLASTIC DIP (300mil)



PACKAGE DIMENSIONS (Continued)

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

Unit (inches)



First-in First-out (FIFO) 2048 x 9 CMOS Memory

FEATURES

- **First-in, First-out dual port memory**
  - **2048 x 9 organization**
- **Very high speed independent of depth/width**
  - **20ns cycle times**
- **Asynchronous and simultaneous read and write**
- **Fully expandable by both word depth and/or width**
- **Low power consumption**
  - **Active: 150mA (max)**
  - **Power Down: 15mA (max)**
- **Half-full flag capability in standalone mode**
- **Empty and full warning flags**
- **Auto retransmit capability in standalone mode**
- **High performance 1.2 micron CMOS technology**
- **Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC**

DESCRIPTION

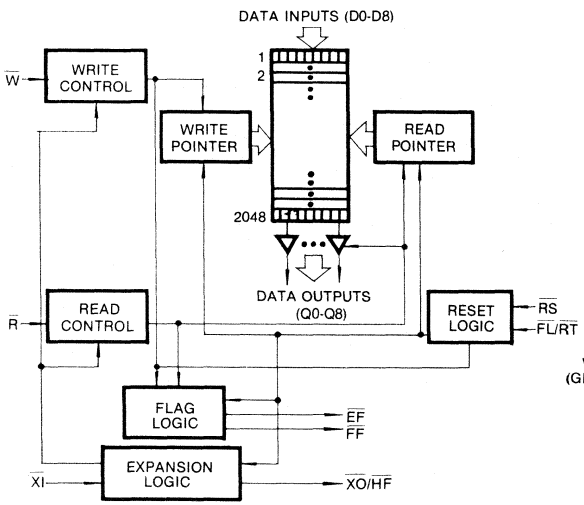
The KM75C03A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

No address information is required for KM75C03A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 20nsec (50MHz).

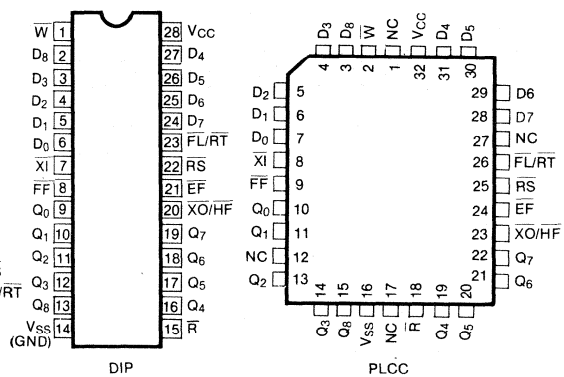
The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

The KM75C03A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_A	0 to +70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%)

Parameter	Symbol	T_A = 15/20ns			T_A = 25ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			150			120	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%)

Parameter	Symbol	T_A = 35ns			T_A = 50ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			100			60	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

Notes: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Measurements with $V_{SS} \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to + 70°C)

Parameter	Symbol	KM75C03A-12		KM75C03A-15		KM75C03A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		30		ns
Access Time	t_A		12		15		20	ns
Read Recovery Time	t_{RR}	8		10		10		ns
Read Pulse Width(2)	t_{RPW}	12		15		20		ns
Data Valid from Read Pulse High	t_{DV}	5		5		5		ns
Read Pulse High to Data Bus at High-Z(3)	t_{RHZ}		15		15		15	ns
Write Cycle Time	t_{WC}	20		25		30		ns
Write Pulse Width(2)	t_{WPW}	12		15		20		ns
Write Recovery Time	t_{WR}	8		10		10		ns
Data Setup Time	t_{DS}	8		10		12		ns
Data Hold Time	t_{DH}	0		0		0		ns
Reset Cycle Time	t_{RSC}	20		25		30		ns
Reset Pulse Width(2)	t_{RS}	12		15		20		ns
Reset Recovery Time	t_{RSR}	8		10		10		ns
Retransmit Cycle Time	t_{RTC}	25		25		30		ns
Retransmit Pulse Width(2)	t_{RT}	15		15		20		ns
Retransmit Recovery Time	t_{RTR}	10		10		10		ns
Reset to Empty Flag Low	t_{EFL}		20		25		30	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		20		25		30	ns
Read Low to Empty Flag High	t_{REF}		20		20		20	ns
Read High to Full Flag High	t_{RFF}		20		20		20	ns
Write High to Empty Flag High	t_{WEF}		20		20		20	ns
Write Low to Full Flag Low	t_{WFF}		20		20		20	ns
Write Low to Half-Full Flag Low	t_{WHF}				25		30	ns
Read High to Half-Full Flag High	t_{RHF}				25		30	ns
Expansion Out Low Delay from Clock	t_{XOL}		16		20		20	ns
Expansion Out High Delay from Clock	t_{XOH}(4)		16		20		20	ns
$\overline{XI}$ Pulse Width	t_{PXI}	12		15		20		ns
$\overline{XI}$ Recovery Time	t_{XIR}	8		10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	8		10		12		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C03A-25		KM75C03A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Access Time	t_A		25		35	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	25		35		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[1]	t_{RHZ}		20		20	ns
Write Cycle Time	t_{WC}	35		45		ns
Write Pulse Width[2]	t_{WPW}	25		35		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	15		18		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	35		45		ns
Reset Pulse Width[2]	t_{RS}	25		35		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	35		45		ns
Retransmit Pulse Width[2]	t_{RT}	25		35		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		35		45	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		35		45	ns
Read Low to Empty Flag High	t_{REF}		25		30	ns
Read High to Full Flag High	t_{RFF}		25		30	ns
Write High to Empty Flag High	t_{WEF}		25		30	ns
Write Low to Full Flag Low	t_{WFF}		25		30	ns
Write Low to Half-Full Flag Low	t_{WHF}		35		45	ns
Read High to Half-Full Flag High	t_{RHF}		35		45	ns
Expansion Out Low Delay from Clock	t_{XOL}		25		35	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		25		35	ns
$\overline{XI}$ Pulse Width	t_{PXI}	25		35		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C03A-50		KM75C03A-80		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	65		100		ns
Access Time	t_A		50		80	ns
Read Recovery Time	t_{RR}	15		20		ns
Read Pulse Width[2]	t_{RPW}	50		80		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		30		30	ns
Write Cycle Time	t_{WC}	65		100		ns
Write Pulse Width[2]	t_{WPW}	50		80		ns
Write Recovery Time	t_{WR}	15		20		ns
Data Setup Time	t_{DS}	30		40		ns
Data Hold Time	t_{DH}	5		10		ns
Reset Cycle Time	t_{RSC}	65		100		ns
Reset Pulse Width[2]	t_{RS}	50		80		ns
Reset Recovery Time	t_{RSR}	15		20		ns
Retransmit Cycle Time	t_{RTC}	65		100		ns
Retransmit Pulse Width[2]	t_{RT}	50		80		ns
Retransmit Recovery Time	t_{RTR}	15		20		ns
Reset to Empty Flag Low	t_{EFL}		65		100	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		65		100	ns
Read Low to Empty Flag High	t_{REF}		45		60	ns
Read High to Full Flag High	t_{RFF}		45		60	ns
Write High to Empty Flag High	t_{WEF}		45		60	ns
Write Low to Full Flag Low	t_{WFF}		45		60	ns
Write Low to Half-Full Flag Low	t_{WHF}		65		100	ns
Read High to Half-Full Flag High	t_{RHF}		65		100	ns
Expansion Out Low Delay from Clock	t_{XOL}		50		80	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		50		65	ns
$\overline{XI}$ Pulse Width	t_{PXI}	50		80		ns
$\overline{XI}$ Recovery Time	t_{XIR}	15		20		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

Notes: 1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

AC TEST CONDITIONS

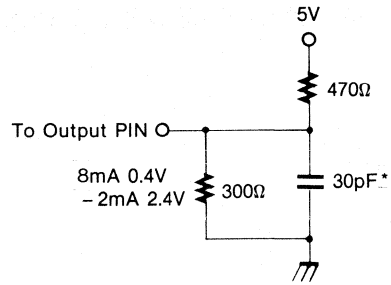
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note: This parameter is sampled and not 100% tested.

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

Note: Generation $\overline{R}/\overline{W}$ Signals-When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

Master Reset ($\overline{RS}$)

Reset is accomplished whenever the MASTER RESET ($\overline{RS}$) input is taken to a low state. During this operation, both the internal read and the internal write pointers are set to the first FIFO location. A Master Reset pulse is required to initialize the FIFO after power-up before any write operation is performed. Both $\overline{R}$ and $\overline{W}$ inputs must be inactive for t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change for t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be set to inactive (high) level after master reset ($\overline{RS}$).

Read Enable ($\overline{R}$)

READ cycles are initiated on the falling edge of the READ ENABLE ($\overline{R}$) input provided that EMPTY-FLAG ($\overline{EF}$) is not low. Read Cycles may be initiated asynchronously to any write operation in progress. After READ ENABLE ($\overline{R}$) goes high, the data outputs will return to a high impedance condition until the next READ operation. If the FIFO is empty, the EMPTY-FLAG ($\overline{EF}$) will go low and prevent any further read cycles. The data outputs will enter the high-impedance state after completion of the last read cycle.

Write Enable ($\overline{W}$)

WRITE cycles may be initiated by a low signal at the $\overline{W}$ input provided the FULL-FLAG ($\overline{FF}$) is not set. Data is stored in the memory array sequentially independent of any read operation that may be in progress.

When more than half of the memory bytes have been filled, the HALF-FULL ($\overline{HF}$) Flag output will be set low and will remain low till the difference between the write pointer and read pointer is less than or equal to one half of the total memory bytes of the device. The HALF-FULL flag is then reset by the rising edge of the read operation.

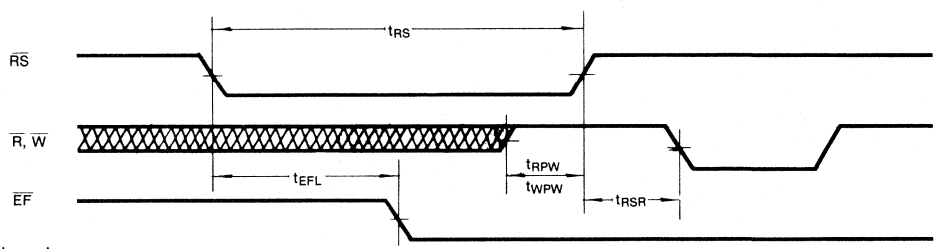
When the memory array is completely full, i.e., when the write pointer is one location from the read pointer, the FULL-FLAG ($\overline{FF}$) will go low preventing any further write operations. The FULL-FLAG will go high again t_{RFF} after completion of a valid read operation.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This input may be used in two different ways depending upon the configuration of EXPANSION-IN ($\overline{XI}$):

1. Single Device or Retransmit Mode: In this mode the $\overline{XI}$ pin must be grounded. Using this mode the device can be used to retransmit data when $\overline{RT}$ is pulsed low. A retransmit operation will set the internal read pointer

Figure 2. Reset



Notes

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{RS}$.

to the first memory location in the array. The write pointer is unaffected. Both write enable and read enable must be inactive during the retransmit operation. This feature is particularly useful for FIFO applications in communications buffers where noise levels may be high and transmission errors are frequently detected. The retransmit feature may not be used along with depth expansion.

2. Depth Expansion Mode: In this mode the ($\overline{FL}/\overline{RT}$) pin is grounded it that device is the first of the "daisy chain." The $\overline{FL}$ pin is kept high if it is further down the chain. For details of Depth Expansion see Operating Modes.

Expansion-In ($\overline{XI}$)

This is a dual purpose input pin. As explained above, $\overline{XI}$ is grounded to indicate single device mode operation. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain" in the Depth Expansion mode.

Full-Flag ($\overline{FF}$)

The FULL-FLAG output goes low inhibiting further write operations when the write pointer is one memory location from the read pointer i.e., the memory array is full. The total length of he memory array is 2048 bytes write operations for the KM75C03A.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This output may be used in two different ways:

Single Device Mode: In this mode this output acts as a HALF-FULL Flag. After half the memory locations are full, and at the falling edge of the next write operation, the $\overline{HF}$ output is set to low. It is reset to high if the difference between the write pointer and the read pointer is half the memory depth or less at the rising edge of the read operation.

Depth Expansion Mode: In this mode EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain." In this way a signal can be passed onto the next device when the current device reaches the last memory location.

FIFO's can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$'s together. $\overline{HF}$ and $\overline{RT}$ functions are available in Depth Expansion Mode.

Single Device/Width Expansion Mode: Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a MR cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFO's can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Figure 3. Asynchronous Write and Read Operation

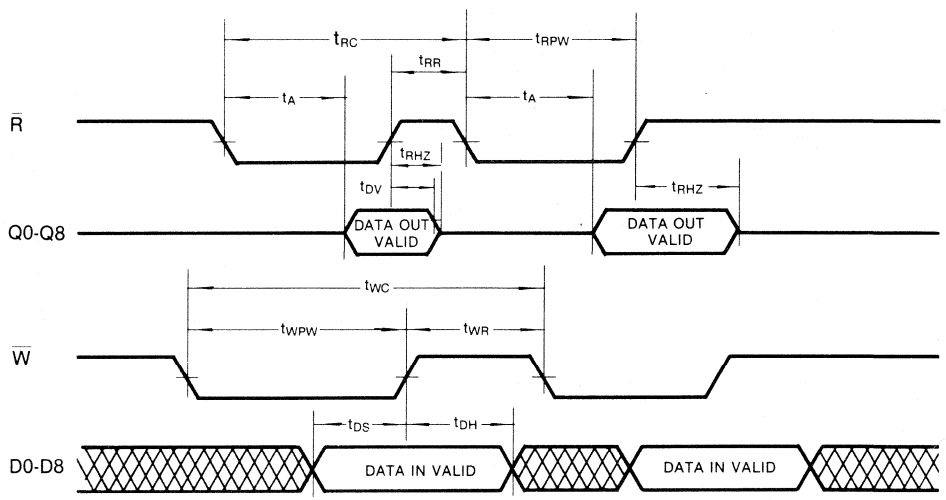


Figure 4. Full Flag From Last Write to First Read

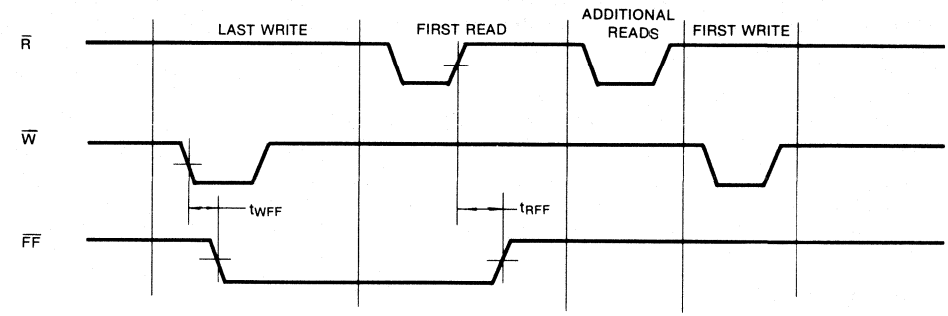


Figure 5. Empty Flag From Last Read to First Write

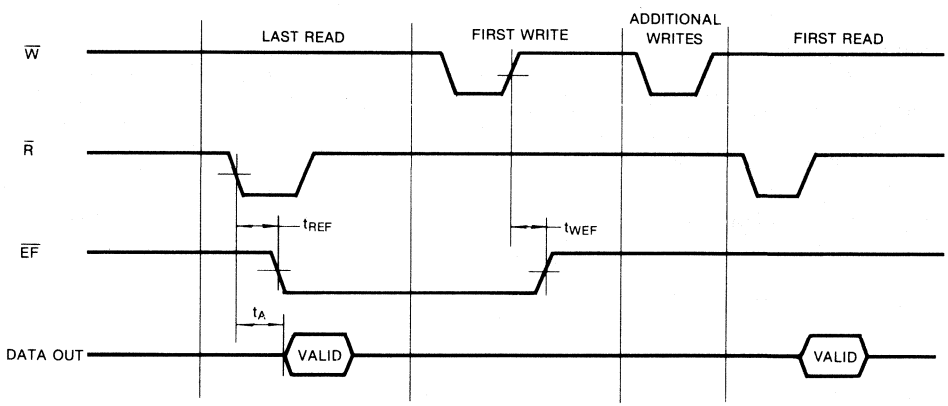
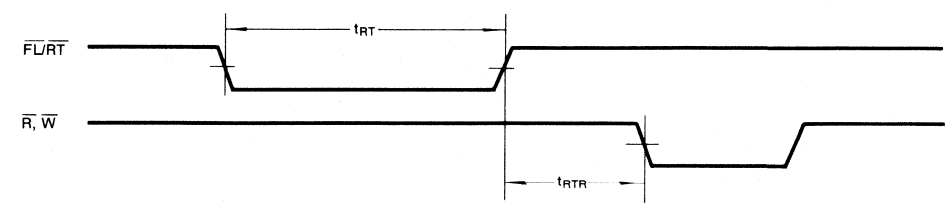


Figure 6. Retransmit



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Expansion-In Timing Diagram

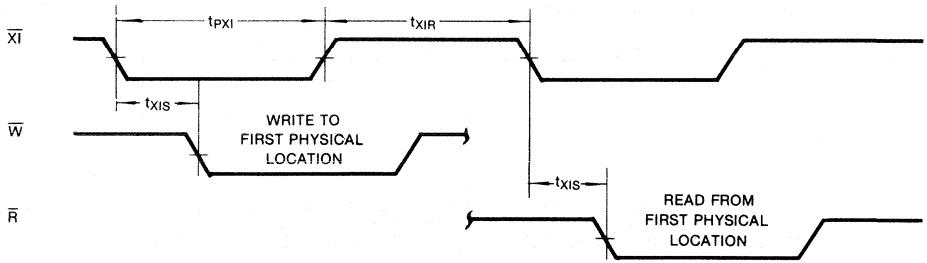


Figure 8. Expansion-Out Timing Diagram

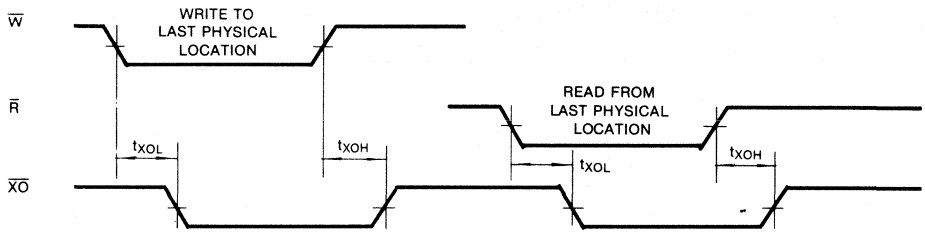
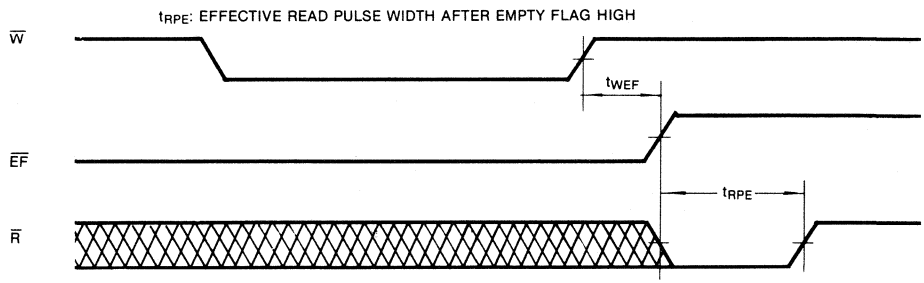


Figure 9. Empty Flag Timing



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 10. Full Flag Timing

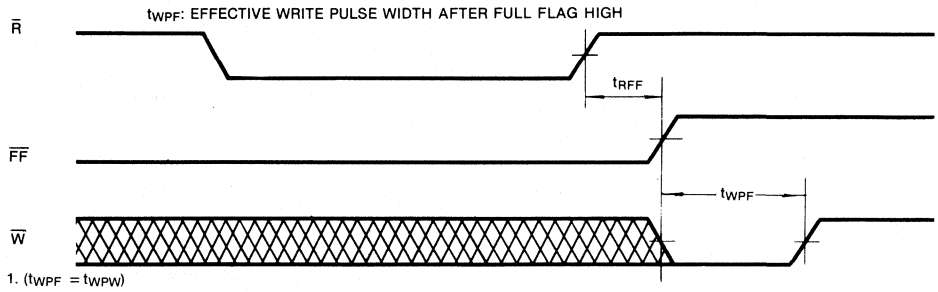
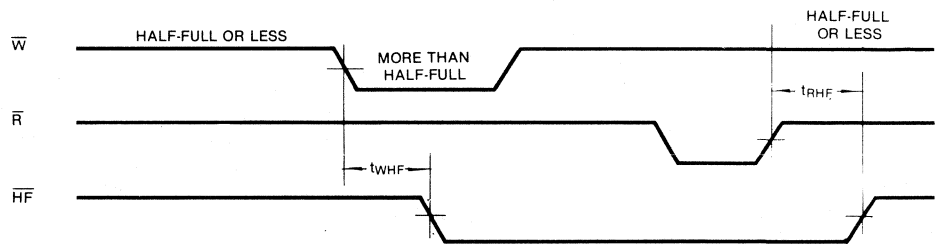


Figure 11. Half Full Flag Timing



OPERATING MODES

Single Device Mode

A single KM75C03A may be used when the application requirements are for 2048 words or less, the device is placed in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded (See Figure 12). In this mode the HALF-FULL FLAG ($\overline{HF}$) and RETRANSMIT ($\overline{RT}$) features are available.

Figure 12. Block Diagram of Single 2048 x 9 FIFO

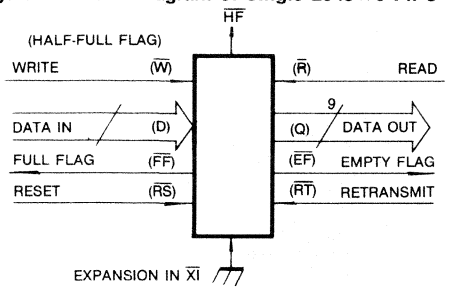
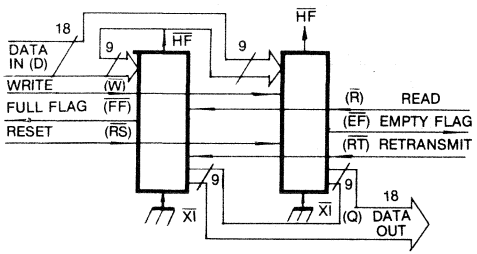


Figure 13. Block Diagram of 2048 x 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two KM75C03A.

Depth Expansion (Daisy Chain) Mode

The KM75C03A can easily be adapted to applications when the requirements are for greater than words. Figure 14 demonstrates Depth Expansion using three KM75C03A. Any depth can be attained by adding additional KM75C03A's. The KM75C03A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input. The RETRANSMIT feature is not available in this mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. The half-full flag ($\overline{HF}$) function is not available in this mode.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (See Figure 15).

Bidirection Mode

Applications which required data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing KM75C03A as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

This section describes two special conditions—when the FIFO is full or empty. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a tri-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the emptly flag); however, the same word (written the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data (from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

TRUTH TABLES

Table 1. Reset and Retransmit-Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1. Pointer will increment if flag is high

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$
Reset	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

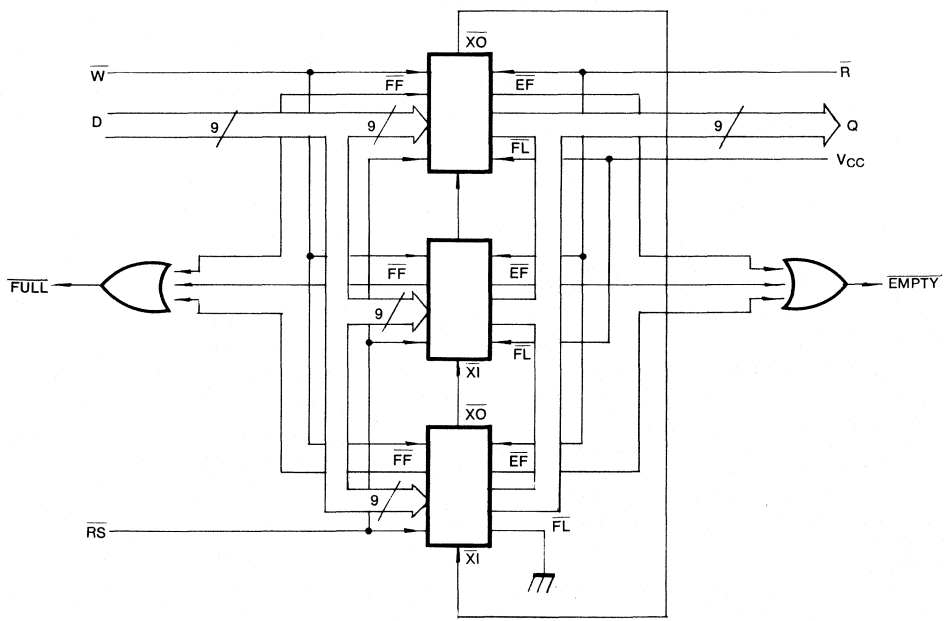


Figure 15. Compound FIFO Expansion

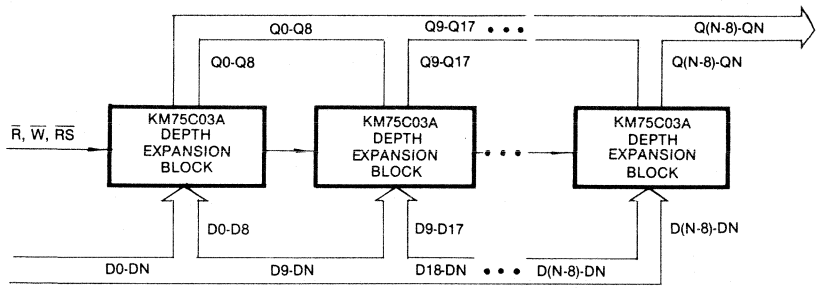
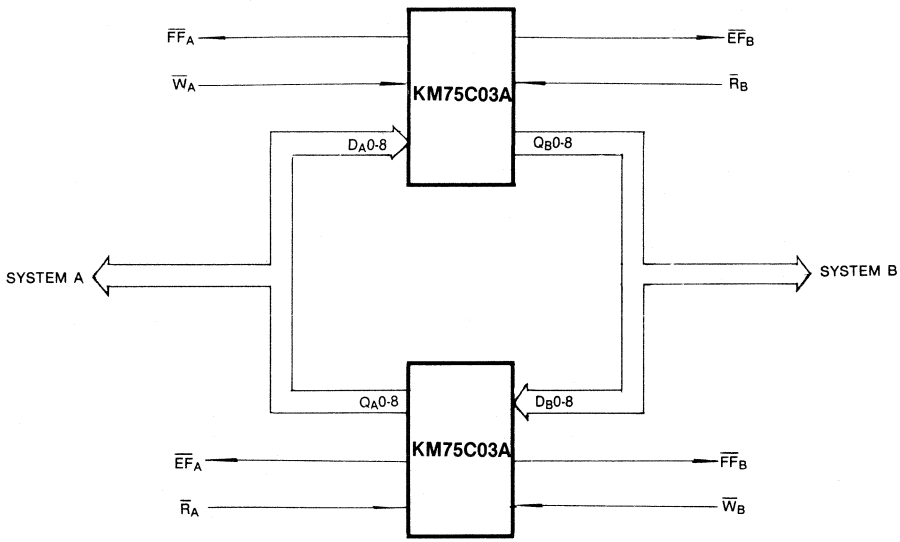
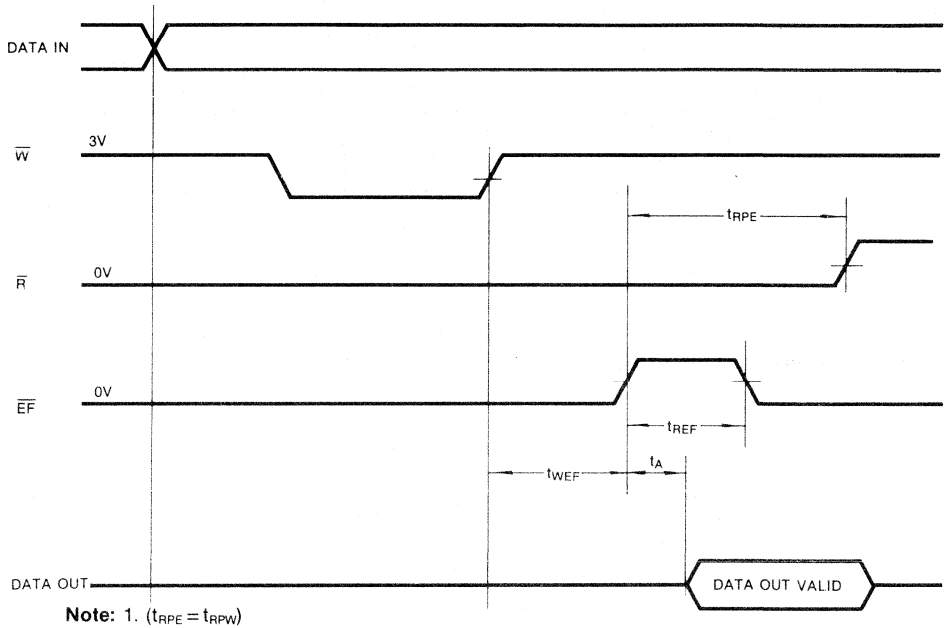


Figure 16. Bidirectional FIFO Mode



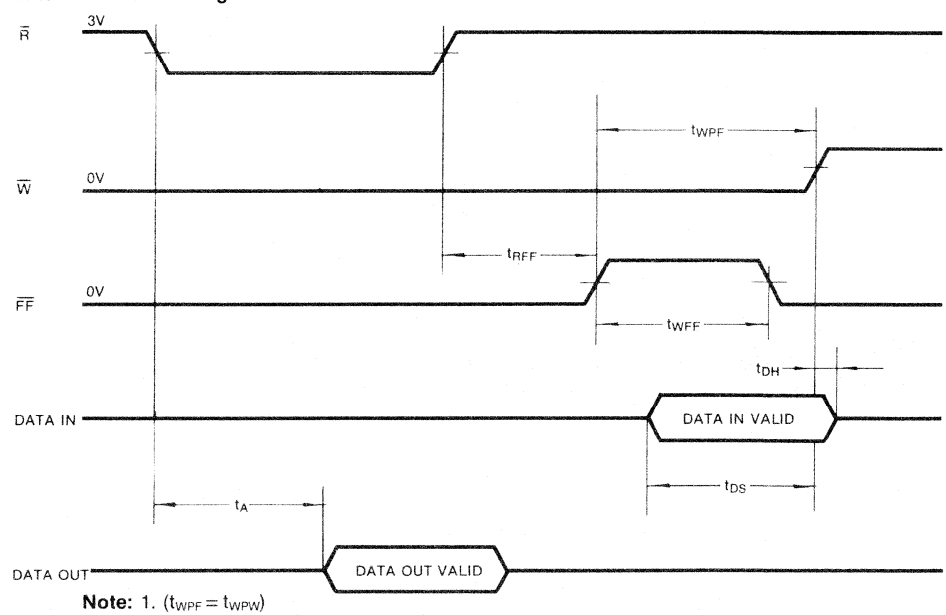
Notes:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 14.
2. For detection see WIDTH EXPANSION Section and Figure 13.

Figure 17. Read Data Flow Through Mode



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 18. Write Data Flow Through Mode

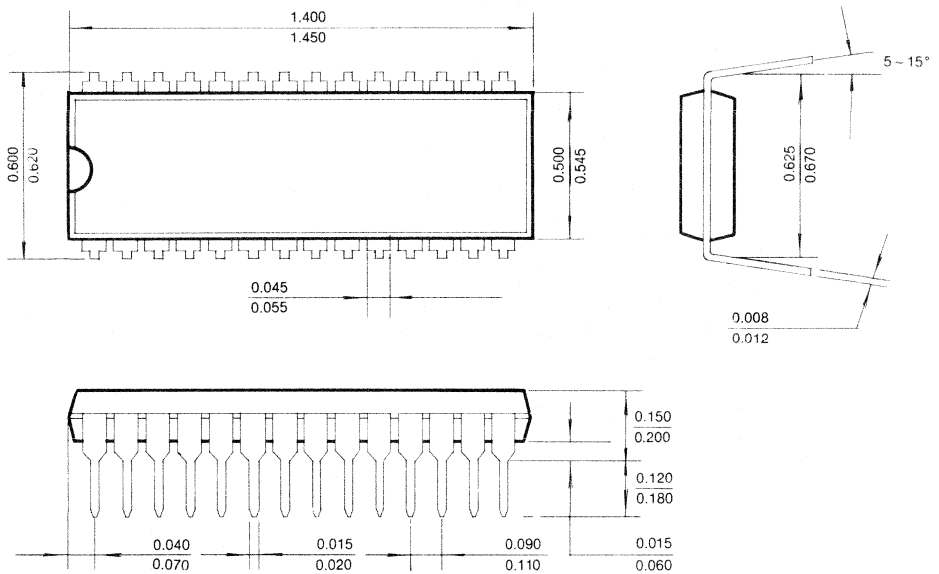


Note: 1. ($t_{WPF} = t_{WPW}$)

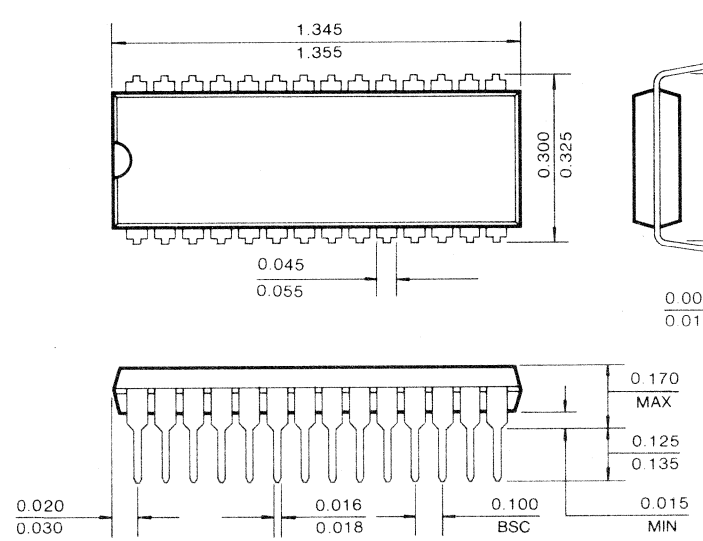
PACKAGE DIMENSIONS

28 PIN PLASTIC DIP (600mil)

Unit (inches)



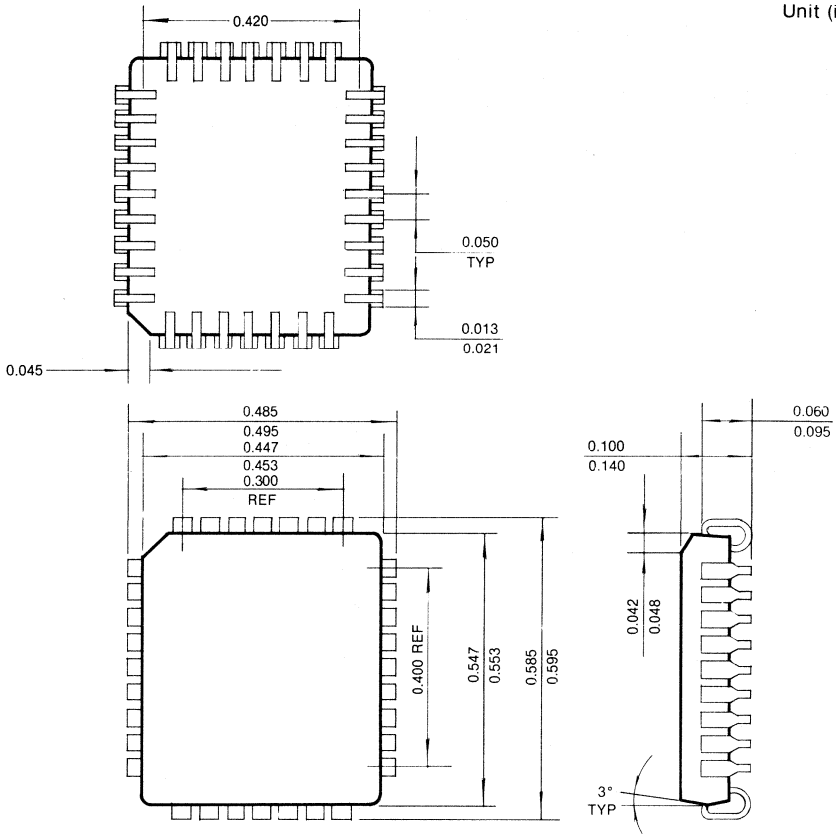
28 PIN PLASTIC DIP (300mil)



PACKAGE DIMENSIONS (Continued)

32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

Unit (inches)



First-in First-out (FIFO) 4K x 9 CMOS Memory

FEATURES

- First-in, First-out dual port memory
  - 4K x 9 organization
- Very high speed independent of depth/width
  - 25ns cycle times
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or width
- Low power consumption
  - Active: 150mA (max)
  - Power Down: 15mA (max)
- Half-full flag capability in standalone mode
- Empty and full warning flags
- Auto retransmit capability in standalone mode
- High performance 1.2 micron CMOS technology
- Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC

DESCRIPTION

The KM75C04A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

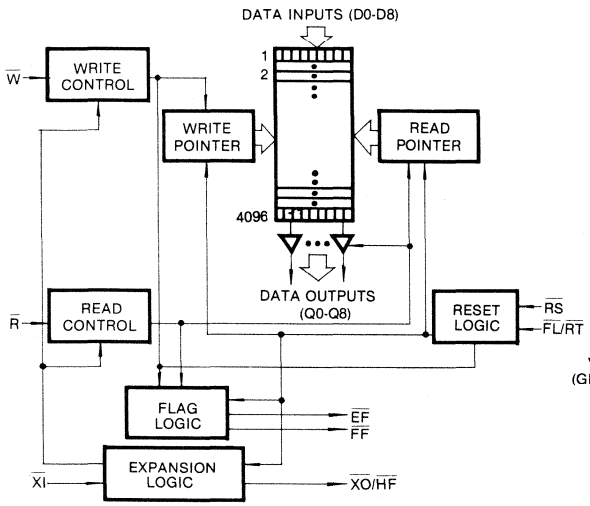
No address information is required for KM75C04A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 25nsec (40MHz).

The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

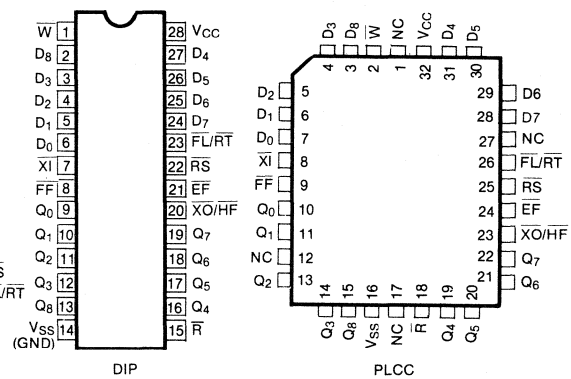
The KM75C04A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

3

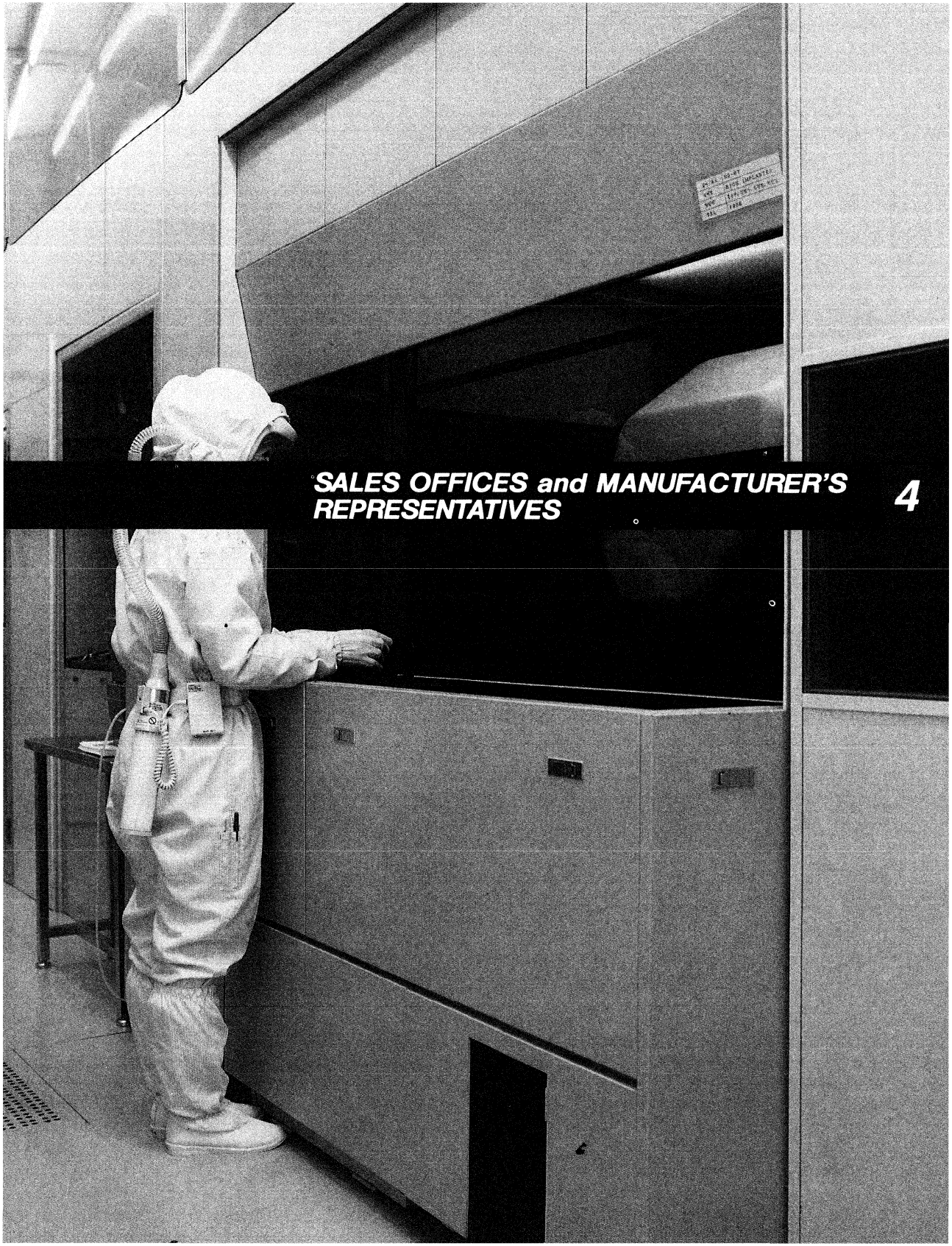
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



NOTES



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